A Hybrid Overload Current Limiting and Short Circuit Protection Scheme for Voltage Mode Inverters

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Abstract- In this study, a current limiting technique which combines an analog comparator circuit and a digital current limiting algorithm is proposed for voltage mode – controlled inverters. Thus, providing smooth output voltage waveform feature of digital current limiting technique and very fast response feature of the analog technique are combined. A three-phase 10kVA voltage mode – controlled inverter has been used to test the performance of the proposed method. Besides, the digital and the analog current limiting techniques have been tested separately to highlight and compare the performance of the proposed hybrid method. It is seen from experimental tests that the proposed technique provides fast response and a successful current limiting performance at short circuit and overcurrent conditions. In addition, the proposed method improves the reliability and fault tolerance capability of the inverter significantly. Moreover, the proposed current limiting algorithm adds fault clearing capability function to the inverter.

Keywords Overcurrent protection; overload; short circuit protection; current limiter; fault-tolerant inverter; voltage source inverter (VSI).

Nomenclature			
VSI	Voltage Source Inverter	V_{ref}	Inverter Output Reference Voltage
UPS	Uninterruptible Power Supply	V_{out_ref}	Digital Current Limiter Input Signal
V_{dc}	Measured DC Bus Voltage	$V_{out\_ref\_limited}$	Digital Current Limiter Output Signal
V_{out}	Measured Inverter Output Voltage	i_{ref_high}	Positive Alternance Analog Current Limit Peak Value
I_{out}	Measured Inverter Output Current	i_{ref_low}	Negative Alternance Analog Current Limit Peak
K_{i_limit}	Digital Current Limiter Parameter	i_{in}	Analog Current Limiter Measured Current
I_{limit}	Digital Current Limit Value		

1. Introduction

The voltage source inverters (VSIs) which are employing several semiconductor power switches, such as IGBTs and MOSFETs are commonly used in industrial applications including the Uninterruptible Power Supplies (UPSs), Distributed Generation (DG) systems, and motor drives [2 – 8]. Among the other causes, power switch faults are the major reason of power circuitry damages. It is reported that about 38% of the faults in a power circuitry of the VSI is due to failures of switching devices [2]. Therefore, designing a proper protection and fault detection system for these inverter circuits is very important requirement to obtain a high-reliability inverter especially for high power systems [2].

UPS applications and stand-alone renewable energy systems are most common voltage mode – controlled inverter applications. Since the UPS's are used to provide uninterruptible power to the critical loads, the reliability of the inverter is very important. Therefore, the protection and fault detection systems employed are one of the major subsystems. Same conditions are also valid for stand-alone inverters supplied by the renewable source and battery back-up. Since the IGBT chip has a finite current capacity, the overcurrent as a result of overload or short circuit operation causes the overheat of the chip. This overheat is the typical reason of the destruction of semiconductor power switches employed in power inverters [3].

The short circuit is one of the most critical conditions to be considered. It may cause serious problems [2, 9]. Different short-circuit protection schemes have been designed and implemented. Using the collector-emitter saturation voltage of the IGBT to detect the short circuit condition is one of these schemes [10]. However, a settling time is required to measure this voltage, and this increases the response time. Typically, it takes about 10 μs to turn off the IGBT with this method. This delay causes severe temperature to raise (about 70°C) in the junction temperature of 1200V rated IGBTs during the short circuit. As a result, the high thermal and electrical stresses destroy the switch [2].

Measuring the device current is another protection method which is used to protect the inverters against the overcurrent and short circuit conditions. In this method, the device current is measured. When it reaches the maximum allowable current value of the device, the protection algorithm is enabled, and the device is turned off [11]. However, turning off the device before it is desaturated may also destroy the device, because the operation point of the device shall be out of its safe operation area (SOA) [2]. Monitoring *di*/*dt* of the device current is another method to protect the device against the short circuit [12]. However, this method suffers from misdetection of short circuit conditions.

Another method employing a protection inductor has been also proposed to protect the device against the short circuit [13]. Although this method provides fast response, additional inductor and thyristor increase the cost and size of the system.

The triple-loop-control algorithm is proposed to limit the overload and short circuit current and provide protection against these conditions. Along with the voltage and current loops, a most inner current hysteretic controller is employed. When the inverter works in normal operation conditions, the third loop does not have any effect on the system. However, when a short circuit is detected and the traditional current controller cannot handle it, the current hysteretic controller limits the current by disabling the PWM pulse. If the preset values are reached, the inverter is shut off immediately [9]. However, as discussed above, immediate turn off the devices, working out of the SOA, may also destroy the switching devices.

This paper has been focused on the overload and short circuit protection of the voltage mode – controlled inverters.

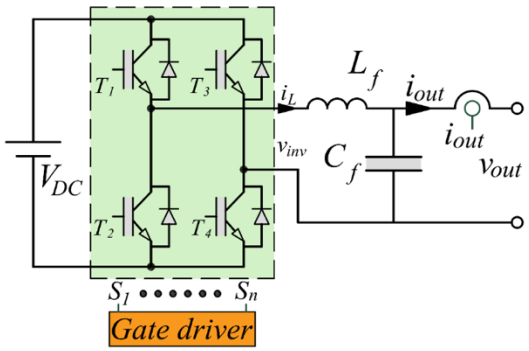


Fig. 1. A general diagram of an DC–AC converter.

The voltage–controlled inverters are commonly used at UPSs and stand–alone renewable energy applications such as photovoltaic systems and fuel cell applications. Since the UPSs are installed to supply the critical loads where the energy continuity is very important, instead of turning the semiconductor devices off, limiting their fault (short-circuit or overcurrent) current is the main purpose of this study. A hybrid model, combining both analog and digital schemes is presented in this paper. Experimental studies have been carried out to test the proposed system for short circuit and over current conditions along with the temporary overcurrent states such as turning on a nonlinear or inrush current drawn load. Analog and digital current limiting techniques are also tested and obtained results are compared with proposed method. The experimental results show that the proposed hybrid method provides better performance even with the low filter inductance value and prevents the destruction of IGBTs.

2. Current Limitation Techniques

Proposed hybrid current limiting technique consist of two parts: A digital current limiting algorithm which can be implemented with a DSP, FPGA or another digital system, and an analog current limiting circuit. Each technique will be discussed separately, and then the proposed hybrid technique combining these two techniques will be explained.

1.1. Digital Current Limiting Algorithm

In Fig. 1, a general structure of a DC – AC converter is given. The digital current limiting algorithm limits the inductor or output current digitally. The algorithm can be applied to different converter topologies including two–level or three–level inverters. Since the algorithm is based on limitation of the control signal, it is independent of the inverter topology.

In Fig. 2 a general control block diagram of an inverter is shown. The current limiting algorithm is placed between controller and PWM modulator. Different algorithms may be used for the inverter control, and it does not have any effect on current limiting algorithm. Current limiter block limits the control signal and acts as a variable limiter for the control signal of the controller. By this way the duty cycle is also limited. Limitation of the control signal is current dependent.

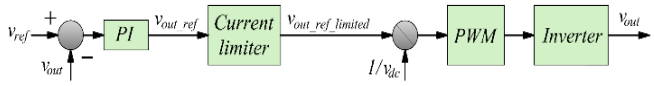


Fig. 2. Inverter control block diagram.

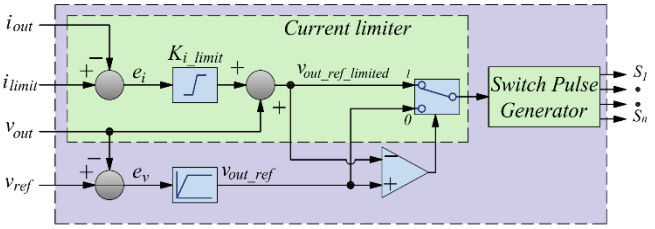


Fig. 3. Detailed block diagram of the digital current limiting algorithm.

The block diagram of the proposed algorithm is given in Fig 3. Interaction of current limiter and control system can be seen in Fig. 3 in more detail. The digital current limiting algorithm is executed at every sampling period together with the voltage control loop. In this way at every PWM cycle current limiting action is obtained. In Fig. 3, V_{out} and I_{out} are real time measured values. I_{limit} and K_{i_limit} are current limiting algorithm parameters.

Equation (1) is implemented as block diagram in Fig. 3 and shows the principle of the algorithm more clearly.

$$V_{out\_ref\_limited} = V_{out} + (I_{limit} - I_{out})K_{i\_limit} \quad (1)$$

Equation (1) generates a variable limiting value for the controller output, depending on the output current. As the output current increases, the limit value decreases. Similarly, as the current decreases, the limit value increases. The switch in Fig. 3 decides if the limiting action will be applied or not. If measured current exceeds the I_{limit} the right-hand side of the (1) becomes negative, and $V_{out\_ref\_limited}$ takes a lower value than the measure output voltage. Thus, the control signal is limited leading a decrease on the output current. If the measured current is below the I_{limit}, then the $V_{out\_ref\_limited}$ takes higher value than the measured output voltage. In this case there will be no limiting in the control signal as well as output current.

K_{i_limit} parameter adds a weighting effect to the algorithm depending on the current. By using K_{i_limit} output voltage oscillations can be minimized during transient (overcurrent or short-circuit) states. Smaller K_{i_limit} values yields more stable output voltage and smaller fluctuations. However, this slew limitation effect has a negative impact on the dynamic response of the voltage controller. Output voltage oscillations and dynamic response are the tradeoffs that should be considered while tuning the K_{i_limit}. In practical implementation, it is seen that K_{i_limit} around 0.1 – 0.8 yields good response for a unity gain control system.

In normal conditions, the current limiter block is at bypassed state. Thus, the limiter has no effect on the inverter regulation. But when an overcurrent occurs, it limits the control signal depending on the current value. From another perspective, at normal current conditions, the inverter is under the control of the inverter regulation and it operates in the constant voltage mode. During overcurrent states, the inverter control signal is limited by the current limiting algorithm leading the transition of the inverter operation to the constant current mode.

1.2. Analog Current Limiting Technique

For fast changing currents such as a short circuit current, the sample-based digital limitation may not be fast enough. Since a short circuit current has a high current changing rate (di/dt), the current may reach dangerous values between two sampling period. For this reason, an analog circuit may be used to detect these types of fast changing currents. An analog circuit can detect signals at continuous time domain. Despite the delay effect of the low pass filters used in the current measurement circuits and delays caused by other non–ideal elements, analog circuits are fast enough to catch the fast–changing currents.

In an AC system, the rising rate of the IGBT current of the inverter at a short-circuit instant depends on the short-circuit occurring angle. If short-circuit occurs when the voltage is small, the short circuit current shall have lower (di/dt). However, if short circuit occurs at the peak of the AC voltage, the current shall have the maximum rise speed (di/dt).

A practical short–circuit case analysis:

For a worse–case scenario, a case in which the short circuit is occurred at the peak value of the inverter output voltage will be discussed. Since short circuit is a very short duration, inverter voltage at the short circuit instant may be assumed as constant. At this instant, the load is short circuited, and the only current limiting element is the filter inductor. In this case, the rising speed of the current depends on the inverter voltage value at the short circuit instant and the inductance value.

Here, a 10kVA, 220VAC inverter with 10kHz switching frequency will be analyzed.

- Since short circuit is an instant and assumed to occurred at the peak, 311V is used as the voltage value during the short-circuit and is assumed as constant.
- A single sampling period for 10kHz system allows maximum 100μs uncontrolled current rise.
- Single-phase power of the inverter is 3.3kW. The Root-Mean-Square (RMS) value of the inverter output current is 15A. The maximum value of the inverter output current is 21A for linear load condition.

For these parameters, the rise rate of the current (di/dt) will be investigated. Another important element of the circuit is the inverter filter inductor. The filter inductor is the only element in the circuit that has a real effect on the current limiting action. Stray inductances and other non–ideal parasitic elements in the circuit has no remarkable effect on the rate of the current rise.

The inductance value of the filter inductor decreases with the increasing current at short circuit conditions. This decrease in filter inductance leads higher di/dt which limits

the current limiting capacity and makes fault current limiting more difficult. Therefore, the current limiting effect of the filter inductor which limits *di*/*dt* of the device current in short circuit conditions should be investigated.

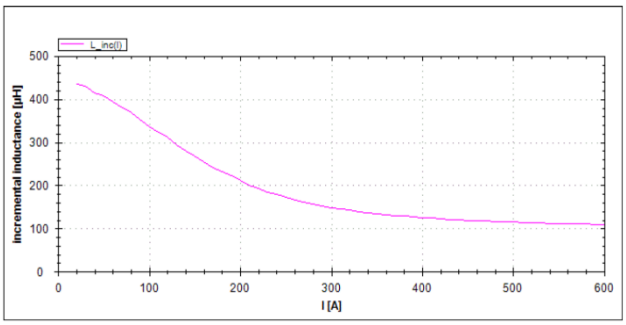


Fig. 4. A sample test results of an inductor with Kool Mμ core.

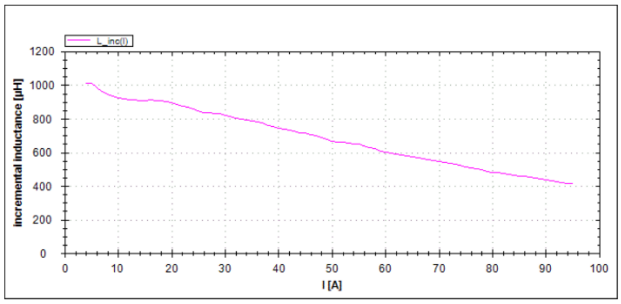


Fig. 5. Test results of the filter inductor used in the experimental tests.

Kool Mμ is a very popular material which is used in high frequency inductors in the industry. It has advantage of being low cost and has low core losses. Although it has good properties, characteristics of a Kool Mμ core inductor significantly changes with the current. As the current increases, the inductance value of the inductor decreases significantly [14]. As discussed earlier, the filter inductance value has a big effect on the rising rate of the current. Smaller filter inductance value leads faster short-circuit current, and this makes the current limiting more difficult.

In Fig. 4 and Fig. 5, characteristics of two different inductors with Kool Mμ cores are given. As it can be easily seen from figures inductance values decreases very significantly with increasing current. If short-circuit occurs just after the current sampling, current shall rise freely depending on the short-circuit voltage and inductance value for $100\mu s$. For worst – case scenario, the Eq. (2) is used to calculate the current.

$$V_{short\_circuit} = L_f \frac{di_{IGBT}}{dt} \quad (2)$$

$$311 = 650\mu H \left(\frac{\Delta i}{100\mu s}\right) \quad (3)$$

$$\Delta i = 48A \quad (4)$$

By using equation (2), (3) and (4), the short circuit current rising is obtained as 48A within a single sampling cycle while the rated current is 21A. In addition, if the inverter is operating at full load, the situation will be worse. The digital algorithm samples the current at 10kHz rate. In this case at the first short circuit instant, digital technique may not detect this fast current and destruction of the IGBT is possible.

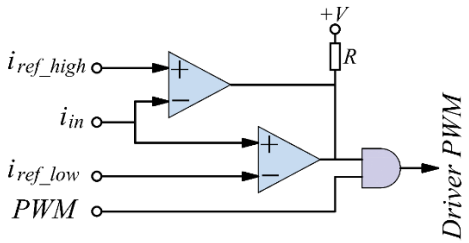


Fig. 6. An implementation of the window comparator circuit for the analog current limiting.

In this study, a window–comparator circuit is proposed to overcome the problem. An analog circuit can detect these types of fast changing currents. In Fig. 6, a window comparator circuit for the analog current limitation is shown. The analog comparator circuits are fast enough to detect short circuit currents. Comparators can detect and respond at a range between nanoseconds to microsecond. Also, the speed of the comparison depends on the voltage difference between comparator inputs called overdrive. The overdrive parameter should be considered when selecting the comparator for this application.

In Fig. 6 the upper comparator is used to detect the positive half cycle of the inverter output current and the lower comparator is used to detect the negative half cycle of the inverter current. In Fig. 6, the system is designed to operate in single supply. Hence, the measured current signal is shifted to positive voltage levels. In Fig. 6, positive half cycle maximum peak current limit value is defined by i_{ref_high}, negative half cycle maximum peak current limit value is defined by i_{ref_low} voltage reference.

If current is outside of the limits, the output of the comparator shuts down PWM signal coming from controller using "AND" gate. Thus, PWM signal to the driver is limited by using comparators. Then, the current shall decrease until the measured current signal to be lower than the hysteresis boundary of the comparators. The hysteresis band of the comparators determines the current ripple caused by analog current limiting. After fault current is decreased to a certain level defined by comparator limits and hysteresis, the drive signals are enabled again, and IGBTs continue their normal operation.

3. Proposed Current Limitation Technique

For VSIs, the limitation of excessive (over-load) and short-circuit currents are very important functions. Even a discharged capacitor or a nonlinear load at the first instant shall behave like a short circuit condition. At the turn on instant, a discharged capacitor operates like a short circuit and draws very high currents which may destroy the switching devices. In addition, a load which includes magnetic components may draw high inrush currents during the magnetization transients. Therefore, employing a fast current limiting function is very important feature for voltage-controlled inverters.

In this study a hybrid current limiting method is proposed. This method combines the analog and digital current limiting methods discussed earlier. In previous sections, both methods are discussed and either method has some disadvantages. By incorporating these two methods together, better current limitation action can be achieved.

In digital current limiting technique, the system operates in constant voltage mode if the current is below the digital current limit. If the current is higher than digital current limit, the system operates in constant current mode. The algorithm performs these transitions automatically. The digital technique has advantage of generating smooth voltage waveform during current limiting. But for fast changing currents, the digital technique may not be able to catch the faults and limit the fault currents. The analog current limiting technique can detect and limit these currents. Unfortunately, the analog technique cannot produce smooth waveforms during current limiting stage when compared to digital technique.

The analog and digital current limiting techniques are employed together to gain advantages of each technique. The reference value for the analog current limiting technique should be set a higher value than the digital current limiting algorithm. In this way, the analog current limiting technique stops the current if the digital technique is insufficient. The analog comparator circuit works at the first instant of the excessive current and then the digital current limiting takes over the control and provides a smooth current limiting waveform.

The inverter and switching devices are immediately protected from the high fault currents by the analog control technique when the digital control is insufficient and fast changing currents are handled. During the current limitation transients, sensitive loads are not affected from inverter voltage distortion because of the smooth current limiting action of the digital technique. In addition, combinational use of the digital current limiting technique yields higher RMS voltage value than the analog technique during the current limiting transients, which is also better for the sensitive loads.

In the experimental part effect of both techniques will be discussed separately, and then combination of the two techniques will be discussed.

4. Experimental Tests and Results

Proposed hybrid current limiting technique is implemented and tested with the three-phase 10kVA inverter. Parameters of the inverter used in experimental tests are given in Table 1. An uncontrolled rectifier with a filter capacitor at its output is defined as a standard nonlinear test load. For testing excessive currents, this standard load shall be used.

First inverter is tested with the standard nonlinear load. In Fig. 7 and Fig. 8, the results obtained from these tests when the digital current limiting technique is employed are given for single-phase and three-phase, respectively. At the first instant, the algorithm is changed the inverter operation mode from the constant voltage mode to constant current mode, and IGBT current is limited successfully. After the first cycle, the nonlinear load capacitors are charged. Then the current decreases and system reaches to its steady state. At the steady state, waveforms become periodical as seen in Fig. 7. The digital current limiting algorithm can be applied to single- or three-phase inverters. Here, all three phases of the three-phase inverter are controlled separately. From Fig. 7 and 8, it is seen that digital current limiting technique provides smooth output voltage waveforms at current limiting duration.

Table 1. Parameters of the inverter used in experimental studies.

Symbol	Value
Output Power, P_{out}	10 kVA
Output Voltage, V_{out}	230 V
Filter Inductor, L_f	900 µH
Filter Capacitor, C_f	20 µF
Switching Frequency, f_{sw}	10 kHz

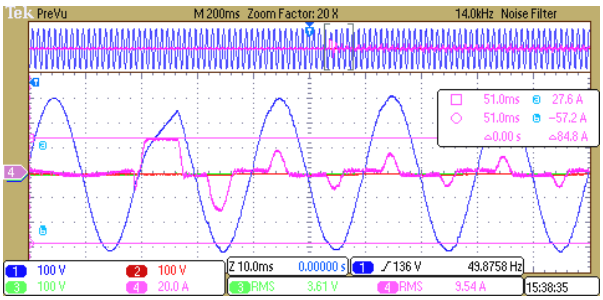


Fig. 7. Performance of the digital current limiting algorithm for nonlinear load.

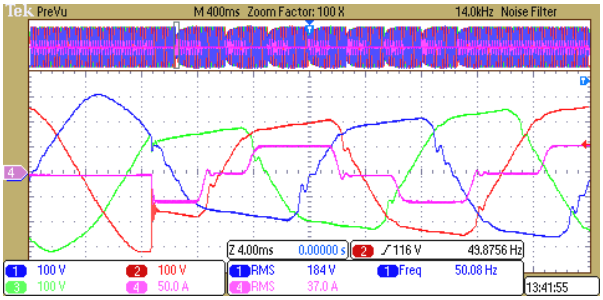
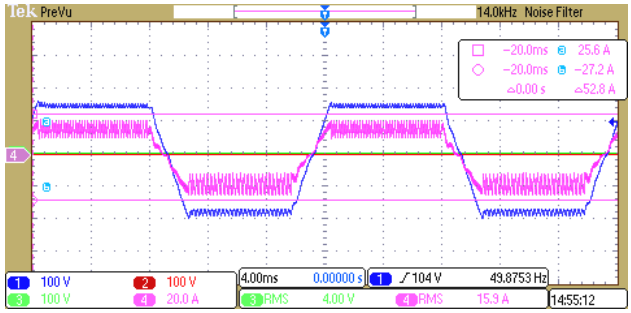


Fig. 8. Performance of the digital current limiting algorithm for three-phase nonlinear load.

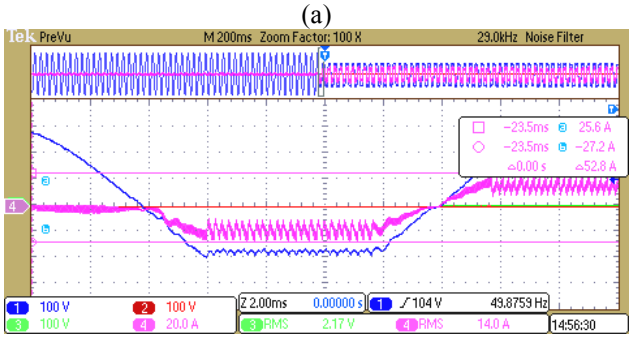
Fig. 9 shows the current limiting response of the analog current limiting technique. The analog current limiting technique successfully limits the overcurrent, but it has much more ripple content compared to digital limiting technique. Besides, the resultant current oscillations cause audible noise in inverter filter inductances. For some applications, the distorted inverter voltage may affect sensitive loads. If the inverter supplies sensitive loads and nonlinear loads at the same time, every transient state caused by overcurrent can disturb sensitive loads. Therefore, use of the analog current limiting alone is not a good solution. In addition to that, analog technique charges nonlinear load capacitance in a

longer time compared to digital technique. Hence, transient state durations are longer in the analog current limiting. These may also have further effect on the sensitive loads.

The hybrid current limiting technique, as mentioned before, combines the analog and digital current limiting techniques to take benefits of both. In the proposed method, the analog limit should always set at a higher value than the digital limit value. In Fig. 10, the analog current limit level is set to 55A whereas the digital limit is set to 18A. As seen from the Fig. 10, at the first instant of the overcurrent, the current is limited at 56A by the analog circuit. After a short duration, the



(a)



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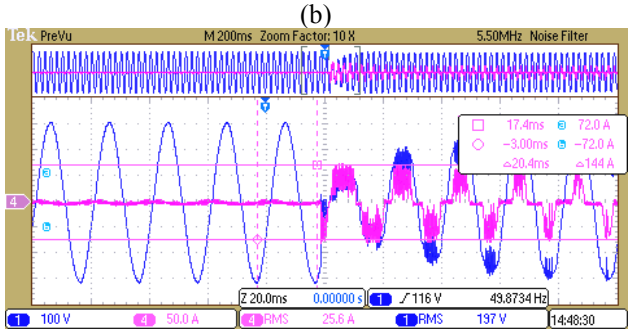

(c)

Fig. 9. Inverter response while the only analog current limiting is active, a) The linear load condition, b) Detailed look of linear load response, c) Nonlinear load condition.

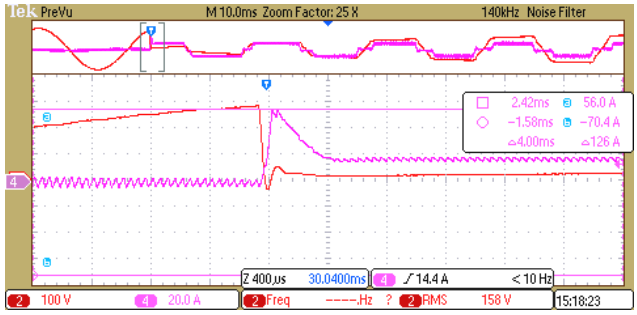

Fig. 10. The current limitation performance of the hybrid current limiting technique with nonlinear load when the the analog current limiting value is set to 55A.

digital technique takes over the control, and the current is reduced to 18A which is the digital current limiting value. To show the current limiting capability of the analog technique, the analog limiting level is reduced to 30A and same test is repeated. Again, the nonlinear load is switched at the peak of the inverter voltage which is the worst case. Fig. 11 shows that the peak overcurrent current is now reduced to 29.6A by analog circuit whereas the digital limit is stayed same as 18A. The nonlinear load tests in Fig. 10 and Fig. 11 are done in the same conditions and at the same angle of the sine wave. According to the experimental results proposed hybrid current

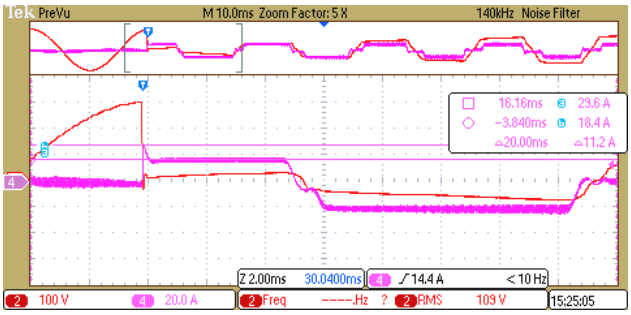

Fig. 11. The current limitation performance of the hybrid current limiting technique with nonlinear load when the the analog current limiting value is set to 30A.

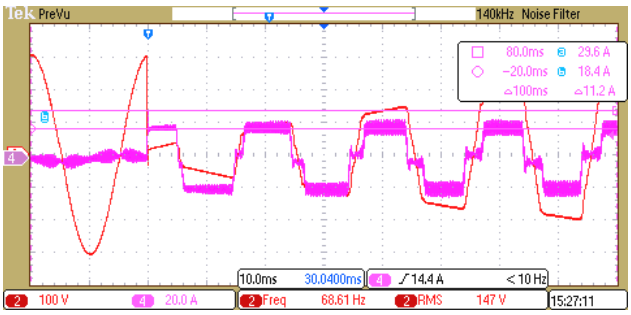

Fig. 12. Current limitation transient with nonlinear load.

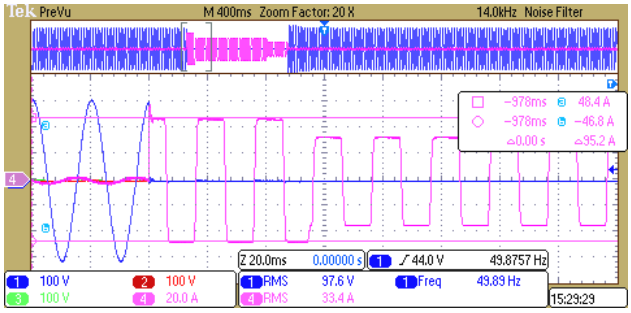

Fig. 13. The limitation of short circuit current.

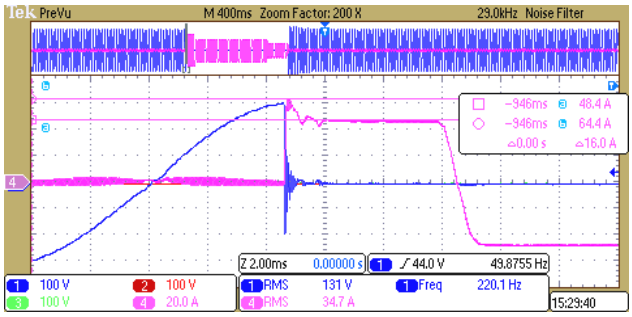

Fig. 14. The fault current when the short-circuit occurs at the peak of the inverter output voltage.

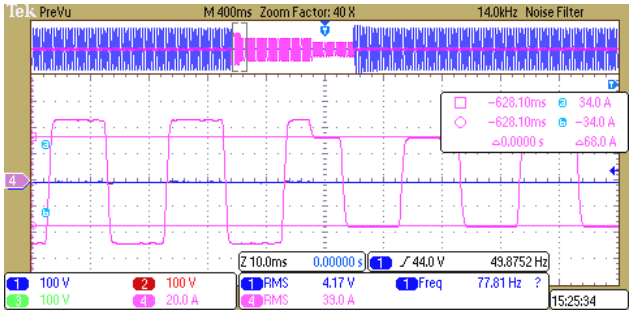

Fig. 15. The effect of short-circuit current set value.

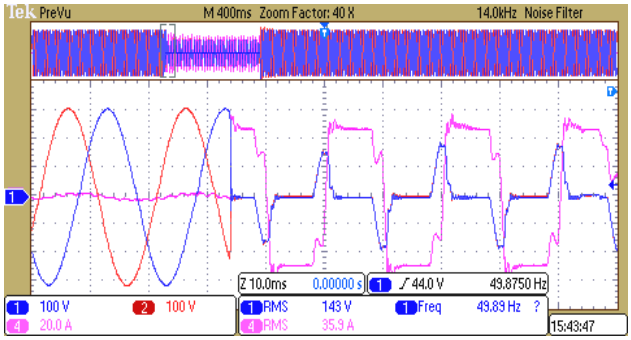

Fig. 16. The limitation of phase-to-phase short-circuit current.

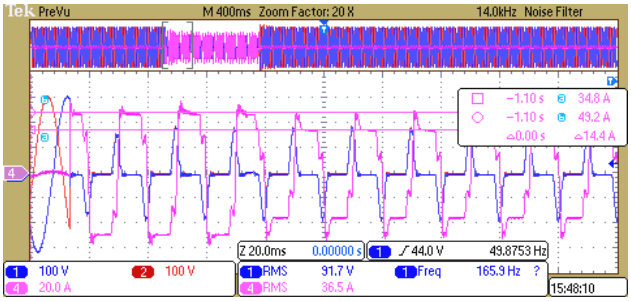

Fig. 17. Changing the current limiting set value during the phase-to-phase short circuit.

limiting technique can stop the current at defined levels and ensures the peak current value never exceeds the upper analog limit. As it is clearly seen in Fig. 12, the proposed hybrid current liming technique provides a smooth voltage waveform at overcurrent conditions and gives fast current limiting capability even at peak voltage short circuits.

Another important overcurrent topic is the short-circuit conditions. The proposed technique can stop overcurrent caused by different types of short-circuits without any modification on algorithm and analog circuit. In Fig. 13, the phase-to-neutral short-circuit test result is given. Before the short-circuit instant, the inverter operates at constant voltage mode. When the short circuit occurs, the inverter switches to constant current mode and output current becomes a square–wave. At the short-circuit condition, the inverter output voltage is nearly zero. It is clearly seen from Fig. 13 that the proposed technique can successfully limit the short circuit. In Fig. 14, the short-circuit duration is zoomed in. The short-circuit condition occurring at the peak value of the output voltage can be accepted as a worst case. It is seen that the proposed hybrid technique can overcome short-circuit events event at the worst case.

The fault current level which will occur at the short-circuit instants can be controlled by changing I_{limit} parameter in the digital current limiting algorithm. Fig. 15 shows the effect of this set value. The set value is decreased at the short-circuit condition and obtained response is depicted in the figure. As seen from the figure, the fault-current is kept at this set value. The heat generated in the semiconductor because of the conduction losses can be minimized by changing the short-circuit current limit level. Usually, cooling fans are supplied by the inverter output voltage. Therefore, fans do not work at short-circuit conditions. Decreasing the short circuit current may be a solution for these kinds of semiconductor heating problems.

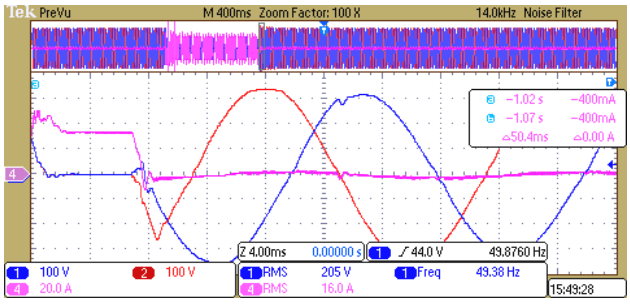

Fig. 18. Transition to normal operation from phase-to-phase short-circuit.

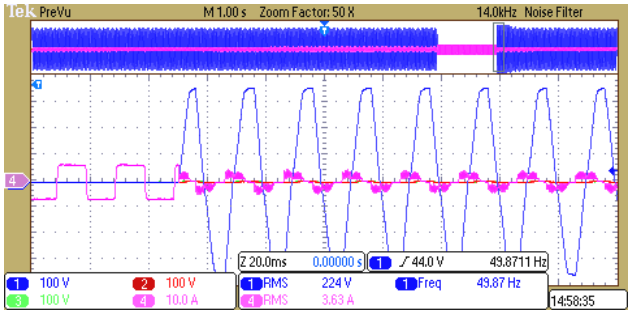

Fig. 19. Transition to normal operation from phase-to-neutral short-circuit.

By using proposed operation method longer short circuit currents can be supplied. In this way, the circuit breakers at the load side can isolate the short–circuited load by removing the fault from the system. Thus, inverter shall continue to supply critical loads with minimum power outage.

In this application, each phase of the three-phase inverter is controlled independently, and each phase has its own analog current limiting circuit. Thus, the inverter is capable of being overcome phase-to-phase short-circuit faults. Fig. 16 and Fig. 17 show the waveforms obtained for phase-to-phase short-circuit fault conditions obtained with the proposed hybrid current limiting technique. Similarly, at phase-to-phase short circuits, the short circuit current can be adjusted by using I_{limit} parameters. In Fig. 17, adjusting the short-circuit current limit value during the fault is seen.

In Fig. 18 and Fig. 19, transition to normal operation (when the short-circuit is isolated) from phase-to-phase short-circuit and phase-to-neutral short circuit conditions are given, respectively. When the short-circuit is removed, the inverter quickly switches to constant voltage mode from constant current mode. These transitions are carried out automatically according to control rule of the digital current limiting algorithm. If inverter voltage regulation algorithm uses an integrator, the value stored in the integrator should be considered after removal of the short circuit, and windup schemes should be employed.

5. Conclusion

A hybrid overload and short circuit protection technique for a voltage–controlled inverter is proposed in this study. The proposed technique combines the analog current limiting technique and the digital current limiting algorithm. Thus, providing smooth output voltage waveform feature of the digital technique and fast response feature of the analog technique are combined. By selecting the proper current limiting value according to the current carrying capability of the switcing devices, the fault current can be kept inside SOA for any conditions with the proposed technique.

Proposed hybrid current limiting technique is tested with 10kVA inverter with linear and nonlinear loads, at phase-to-neutral and phase-to-phase short-circuit conditions. Experimental results validate that the proposed technique provides fast and stable response, prevents destruction of semiconductors during fault instants. and improves system reliability significantly. Besides, it allows to use lower filter inductance values and thus helps to decrease on system cost and size. The proposed current limiting algorithm is easy to implement and easy to understand. Parameters of the algorithm is also easy to tune. The algorithm has no effect on the inverter voltage regulation under normal conditions and it shows effect on the control path only at overcurrent situations. Therefore, the proposed algorithm can run together with different voltage regulation algorithms.

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