Super Twisting Algorithm Based Sliding Mode Controller for Buck Converter Feeding Constant Power Load

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Abstract- When the power electronic converters in the DC microgrid structure are connected in a cascade structure, they may exhibit constant power load (CPL) behavior. CPL's negative incremental impedance causes an unstable influence on in DC microgrid. However, by employing various control strategies, these systems may be made stable. When compared to traditional control methods, sliding-mode control, which is a non-linear control approach, provides a more robust response to external disturbances. In this paper, the performance of a conventional sliding-mode controller for a DC/DC buck converter feeding a CPL is improved using the super twisting algorithm. The super twisting method, which is a second-order sliding mode control algorithm, is a technique used to decrease the chattering effect of the sliding mode controller. In the proposed method, the switching rule of the conventional sliding mode control has been changed by adding super twisting control law. The proposed controller guarantees system stability during steady-state and ensures that the output voltage stays constant whether the input voltage or constant load power changes. Also, the proposed controller greatly decreased the chattering effect, which is the most major drawback of sliding mode control. The performance of the proposed controller was verified by both simulations in the MATLAB/Simulink and experimental studies. Moreover, the superiority of the proposed controller was offered by comparing it with the conventional sliding mode control.

Keywords multi-converters, super twisting algorithm, constant power load, DC microgrid, sliding mode control.

1. Introduction

The energy industry is currently dealing with a slew of issues, including rising energy costs, outdated infrastructure systems, preserving power quality, ensuring continuity, global warming, and climate change. Therefore, many countries are investing in clean and novel energy types to alleviate environmental issues. Microgrids are viewed as a solution to today's environmental problems since they enable the use of renewable energy sources such as solar and wind etc. As a result, the use of microgrids has increased dramatically in recent years [1].

The microgrid is a small-scale power grid that can operate together with or independently of the main grid [2]. As shown in Fig. 1, microgrid comprises many components such as renewable energy sources, energy storage systems, power electronic converters, and loads [3]. There are also novel generation loads, such as electric vehicles, constant power loads (CPL) in microgrid structures [4]. Today, the interest in DC microgrids is growing for a variety of reasons, including energy efficiency, ease of control, and a lack of frequency and reactive power components [5]. Despite these advantages, stability is the main problem of DC microgrid, especially due to constant power loads. CPLs have negative impedance characteristics. Such loads have a devastating impact on the microgrid's stability [6]. As a result, as the proportion of CPLs in the microgrid increases, the stability issue has become more severe [7].

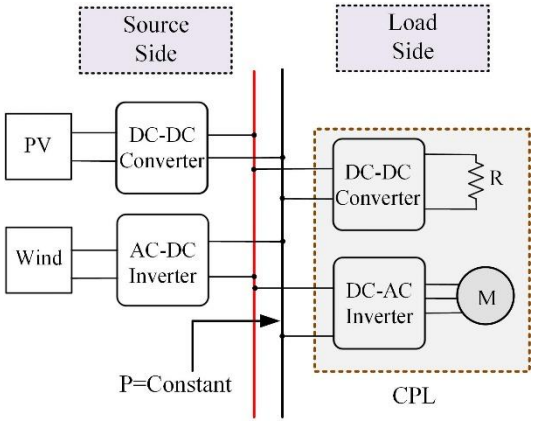

Fig. 1. DC microgrid with CPL

A large number of DC/DC converters are interconnected in various (series, cascade, and parallel) structures in DC microgrid systems These structures are also called multi-converter power electronic systems [8]. The design of the simplified converter system connected in a cascade structure used in the DC microgrid is shown in Fig. 1. As seen in Fig. 1, the converter on the load side can act as a CPL in a cascaded structure, although it can operate stably while feeding a load alone. The first is referred to as a source converter or upstream, while the second is called a load converter or downstream. While the source converter supplies power to the common bus and regulates the voltage, the load converter transmits the power it receives from the bus to the loads. When the output of the load converter is tightly regulated and controlled, the load converter behaves as CPL [9]. In CPL behaviour, while the instantaneous value of impedance is positive, its change is always negative. Therefore, the voltage decreases as the current increases, or the voltage increase as the current decreases to achieve the constant power demanded by CPL [10]. The effect, in this case, is known as the negative impedance effect, and the instability that occurs in the system is called negative impedance instability. Because of the negative incremental impedance property of CPL, voltage sags, oscillations, and instabilities have occurred in cascade converter systems. As a consequence, a robust, fast-response, and low-cost control approach should be devised to assure the stability of microgrid systems.

Many researchers have designed linear control-based solutions to overcome the CPL instability issue. A.M. Rahimi et al. has recommended an active damping method based on the virtual resistance addition method for basic DC converters that supply in [11]. In [12-14] different active damping methods were used to provide constant power to the CPL. In a cascade structure, an LC filter, a voltage source, and a CPL were connected, and the stability of the system was provided by adding passive elements [15]. Increasing the number of passive elements, on the other hand, has increased the system's size, cost, and weight. Furthermore, more energy has wasted. Classical linear control approaches that include control loops or passive elements haven't completely solved this problem [16]. The stability of system is attempted to be provided only around a certain point. Also, these methods are limited in their ability to respond to external disturbances, voltage, and power changes. The main disadvantage of linear control methods is that they cannot ensure the global stability of the intended equilibrium point.

Converters are elements that exhibit nonlinear behaviour. When multi-converter systems supply a CPL, the nonlinearity of the system increases further due to CPL. Nonlinear control methods such as sliding mode control (SMC), passivity-based control, fuzzy logic, etc. for converter systems feeding CPL have been presented by the authors in the literature. M. Al Nussairi et al. proposed a fuzzy logic controller to solve the CPL problem in a cascade converter system [17]. It is determined that SMC is one of the most convenient methods for the CPL problem [18]. The SMC gives robust results against load changes and external disturbances [19]. Researchers especially emphasized the aspects of SMC such as ease of use, simple structure and mathematical demand for less processing. SMC is an advanced nonlinear control method that is fast, stable, and easy to implement [20]. A. Emadi et al. designed a SMC with a simple structure for the buck converter running CPL in [8]. However, this controller can't exactly provide voltage regulation exactly within the DC microgrid. D. Fulwani et al. designed a SMC using a non-linear surface for the boost converter with CPL [21]. The authors in [22] designed a SMC with integral for stable operation of a CPL supplied by DC/DC converter for use in ship DC power systems. In [23], the proposed SMC controller outputs that were directly utilized as gate signals, was used to generate pulse width-modulated (PWM) gate signals for the DC/DC converter. In [24] H. Lin et al. introduced an observer-based adaptive SMC to stabilize the boost converter that feeds a resistive load connected in parallel to the CPL. The proposed method maintains the robustness against external disturbances thanks to its structure, but the observer design is quite complex. Martinez-Trevio B.A. et al. investigated a simplified model of the cascade connection of two DC-DC switching converters using SMC theory principles [25]. A high-order sliding mode controller for the CPL instability problem is suggested in [26].

In the literature, conventional first-order sliding mode control (SMC) methods are generally preferred. The most important shortcoming of the SMC, which stands out in the previous studies, is the steady state error and chattering effect [26]. The Super Twisting Algorithm (STA) method, which is the high-order sliding mode control algorithm may alleviate SMC drawbacks such as relative degree restriction and chattering effect [27]. As a result, a STA-based control rule was proposed by changing the control rule of SMC.

In this paper, STA-based SMC was designed for a DC/DC buck converter feeding CPL. Although STA is a high-order SMC algorithm, it is used in the first-order sliding mode control rule in this study. Conventional SMC's control rule (u) is the sum of the equivalent control rule (u_{eq}) and the discontinuous control rule (u_{sw}). In SMC, the discontinuous control rule causing chattering effect was removed and the STA algorithm was used instead. It was shown that the proposed control rule provides precise stability. Furthermore, the STA-SMC only is followed the output voltage based on the reference voltage. The switching signal obtained from the output of the controller can be used directly for PWM without

the need for extra processing. The advantages of the proposed controller were shown by comparing it with the conventional SMC. The performance and dynamic responses of the proposed controller were investigated in simulation studies built-in Matlab/Simulink environment. It was verified by simulations that the designed controller gives robust and dynamic responses to external disturbances under different operating conditions. Furthermore, the simulation results for the STA-based SMC were validated using the results of the laboratory experiments. The test results obtained studies for several cases show that the proposed controller gives a very fast and robust dynamic response when any deterioration occurs in the input voltage or CPL power. Furthermore, when compared to conventional SMC, the STA-based SMC method significantly reduces the chattering effect and steady-state error.

The rest of this paper is as follows: CPL equivalent models and the stability analysis of a cascade DC/DC buck converter feeding CPL are performed in section II. In section III, the SMC methods are briefly mentioned. Section IV explains the STA-SMC planning procedure for the buck converter feeding CPL. Section V offered both simulation studies and experimental studies. The proposed controller has been tested during several external disturbances that occurred in the input voltage, CPL power, and reference voltage. Finally, conclusions are presented in section VI.

2. Instability of Buck Converter Feeding CPL

2.1. CPL Equivalents Models

The CPL, in contrast to a resistive load, is a non-linear load with negative incremental impedance. As a result of the constant power demand, if the CPL input current increases, the input voltage decreases, or if the input current decreases, the input voltage applied to the circuit increases. Fig. 2 shows the voltage-current characteristic of the CPL, which demonstrates its negative impedance property. The instantaneous value of the load impedance is positive in Fig. 2, but the rate of change of voltage and current is always negative. If there is a disturbance at the cascade converter system's input or the power of the load, the system will move away from the operating point and fail to return to the point where the cascade converter system works stable. When a failure occurs while a system is running stably, it should be able to return to its stabilization point. However, due to negative incremental impedance, CPL feeding cascade converter systems experience negative impedance instability [28].

The CPL design in the nonlinear model is made using Eq. (1) [7]. Where ε is a small positive value. To use linear control methods, a small-signal model (linear equivalent model) should be extracted by performing specific stability points.

$$i(t) = \frac{P}{v(t)}, \quad \forall\, v(t) \geq \varepsilon \tag{1}$$

Moreover, the negative impedance effect is obtained through linear model operations. Small-signal analysis (SSA)

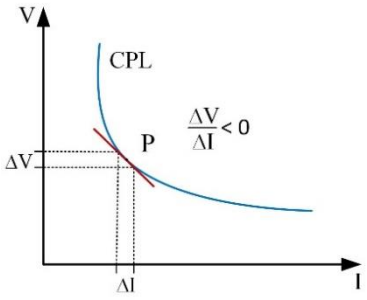

Fig. 2. CPL negative incremental impedance

can be used in such cases. SSA is an analysis method for linearizing nonlinear elements around a point. To obtain a linear CPL model, "*P*" point in the voltage-current characteristic shown in Fig 2 can be applied SSA. Then CPL's current value is as follows:

$$\Delta \boldsymbol{i} = \frac{\boldsymbol{d}\left(\frac{\boldsymbol{P}}{\boldsymbol{v}}\right)}{\boldsymbol{dv}} \Delta \boldsymbol{v} + \frac{\boldsymbol{d}\left(\frac{\boldsymbol{P}}{\boldsymbol{v}}\right)}{\boldsymbol{dP}} \Delta \boldsymbol{P} \tag{2}$$

$$\hat{\imath} = -\frac{P}{V^2}\hat{v} + \frac{\hat{p}}{V} \tag{3}$$

$$R_{cpl} = -\frac{V^2}{P} \tag{4}$$

Based on Eq. (3), a linear equivalent model of the CPL can be formed by connecting a resistor parallel to a current source. Equation (4) shows that CPL has a negative impedance. The CPL linear equivalent model is depicted in Fig. 3a. Fig. 3a shows that the current source does not affect stability. However, since the CPL's negative impedance effect decreases the converter's input impedance on the load side, it induces instability in the cascade converter system.

The model obtained from the large-signal analysis is used to solve the CPL problem using nonlinear control methods. The CPL can be modeled as a dependent current source [29]. The CPL large-signal model is depicted in Fig. 3b.

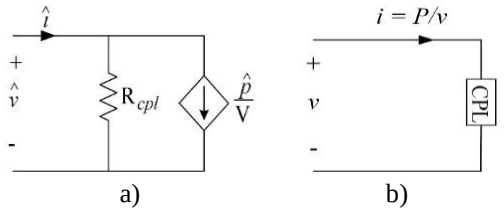

Fig. 3. CPL equivalent models a) small-signal model b) large-signal model

2.2. Stability Analysis

Fig. 4 illustrates a simplified buck converter circuit with CPL in DC microgrid. Consider a buck converter in continuous conduction mode that has been loaded with a CPL, as is depicted in Fig. 4. Based on the on and off states of the switch, the following state-space equations of the source converter are defined to construct the controller.

Switch on (0 < t < dt):

$$\frac{di_L}{dt} = \frac{v_{in}-v_o}{L} \quad (5)$$

$$\frac{dv_o}{dt} = \frac{v_{in}}{C} - \frac{P}{Cv_o} \quad (6)$$

Switch off ($dt < t < T$):

$$\frac{di_L}{dt} = -\frac{v_o}{L} \quad (7)$$

$$\frac{dv_o}{dt} = \frac{v_{in}}{C} - \frac{P}{Cv_o} \quad (8)$$

The values are represented as i_L inductor current, v_o the output voltage, P CPL power, v_{in} the input voltage, L inductor, and C capacitor. The control signal obtained for the switch is denoted by "u". The duty ratio of the converter is indicated by "d", and the switching period is denoted by "T" The buck converter's dynamic model is built using the state-space averaging approach:

$$\frac{di_L}{dt} = \frac{v_{in}}{L}u - \frac{v_o}{L} \quad (9)$$

$$\frac{dv_o}{dt} = \frac{i_L}{C} - \frac{P}{Cv_o} \quad (10)$$

Eqs. (9) and (10) are valid only if;

$$i_L > 0,\ v_o > 0 \quad (11)$$

The system's equilibrium point (x_e) with a constant duty cycle (d) are as follows:

$$x_e = \begin{pmatrix} I_L \\ V_o \end{pmatrix} = \begin{pmatrix} \frac{P}{V_o} \\ V_{in}D \end{pmatrix} \quad (12)$$

Conventional studies of constant power load behavior usually depend to an analysis by linearizing. The negative impedance is defined in the linearized model. However, Eq. (10) is nonlinear system due to the nonlinear characteristic of the CPL. Thus, the global system behavior is more complicated. Depending on the initial conditions of inductor current and capacitor voltage, as well as the power value, the system can exhibit limit-cycle behavior [30].

By selecting u=0 in Eq. (9), the dynamic model of the buck converter feeding the CPL is derived as follows:

$$\frac{di_L}{dt} = -\frac{v_o}{L} \quad (13)$$

$$\frac{dv_o}{dt} = \frac{i_L}{C} - \frac{P}{Cv_o} \quad (14)$$

Fig. 5 depicts the dynamic behavior of Eqs. (13) and (14) through phase portrait using the values listed in Table 1. In Fig. 5, the purple line is the load line of the CPL; the blue line is the trajectory of the state variables. The trajectory's changing direction is indicated by the black arrow.

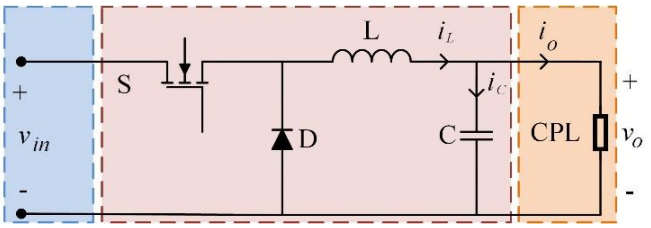

Fig. 4. Buck converter feeding CPL

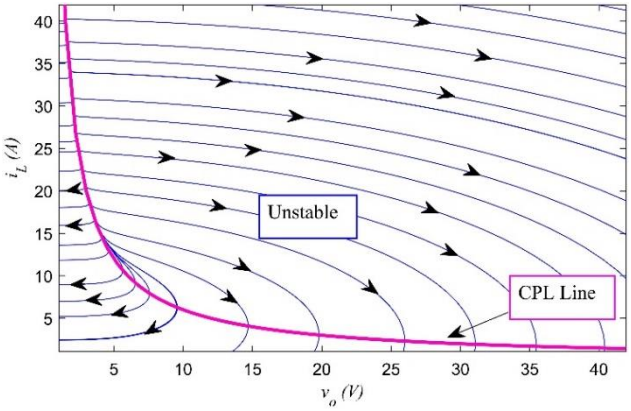

Fig. 5. Phase portrait of buck converter feeding CPL, u =0

It can be seen from Fig. 5 that the trajectory will cross the CPL line and go to the region below the CPL line if the state variable is above the CPL line (purple line). If the state variables are below the CPL line, eventually, the trajectory will become $v_o = 0$ and $i_L = 0$. As a result, when u = 0, the buck converter feeding CPL is unstable throughout the whole phase plane.

By selecting u=1 in Eq. (9), the dynamic model of the buck converter feeding the CPL is derived as follows:

$$\frac{di_L}{dt} = \frac{v_{in}}{L} - \frac{v_o}{L} \quad (15)$$

$$\frac{dv_o}{dt} = \frac{i_L}{C} - \frac{P}{Cv_o} \quad (16)$$

Its phase portrait is shown in Fig. 6. The separatrix (the yellow line), as illustrated in Fig. 6, divides the state plane into two sections. As seen in Fig. 6, the left region of the separatrix is an unstable region, and the right region is a stable region. Furthermore, the trajectory will converge to a limit cycle (the red line), when the state variable is in the stable area.

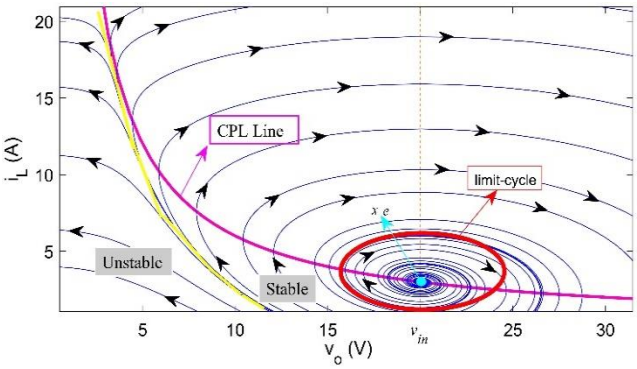

Fig. 6. Phase portrait of buck converter under CPL when u =1

In both situations (u=0 and u=1), the unstable mode and the limit cycle mode, are undesirable in most applications. Therefore, the aim is to design a controller that regulates state variables to a point of equilibrium.

2. Sliding Mode Control

Linear control techniques are utilized to regulate DC/DC converters in the majority of applications. Traditional linear control techniques cannot, on the other hand, completely overcome the CPL's instability. Linear compensation techniques, such as passive and active damping are susceptible to external disturbances as well. SMC, a nonlinear control technique, is one of the best options for this problem [31]. It has many superior characteristics, such as robustness against external disturbances affecting the system, insensitivity to parameter changes, quick dynamic response, ease of application, and adjustment. The SMC method for a system is designed to direct the states of the system to a special surface called the sliding surface in the state space. When the designed controller reaches the sliding surface, it attempts to maintain the system states on the sliding surface using the determined control law. Therefore, SMC consists of two design phases. First of all, a sliding surface must be defined, and the second is a control law, which transfers the state of the system to the surface. The section that passes until it reaches the sliding surface is called the reachability phase. The system is sensitive to external influences in this phase. Then, the slide phase begins when it reaches the sliding surface. The system is robust against disturbances as it uses the equations of the control rule in the sliding phase. However, chattering and relative degree restriction occurs in the conventional SMC (or first-order SMC) technique. Chattering is a drawback because it is caused by unwanted and uncontrollable high-frequency waves that slide in a zig-zag pattern in the state variables. High order sliding mode control (HOSMC) designs remove drawbacks such as chattering and relative degree constraint while retaining the benefits of conventional SMC. The main purpose of the HOSMC method is not only to drive the sliding function (σ) to zero but also to try to zero successive derivatives of the relative degree (r) of the sliding surface relative to the control input. It is expressed mathematically as follows [32]:

$$\sigma = 0, \dot{\sigma} = 0, \ddot{\sigma} = 0 \dots \dots \dots \dots \sigma^{r-1} = 0 \quad (17)$$

Second-Order SMC (SOSMC) is used when the system's relative degree is two. Twisting, super twisting algorithm (STA), sub-optimal, quasi-continuous, and drift are some of the most well-known SOSMC algorithms. This STA does not use the sign function in the sliding function and does not require the sliding function's first derivative. It is also possible to use fixed switching frequencies. For the STA to be valid, the relative degree must be one. In other words, once the sliding function's derivative is determined, the switching input *"u"* must be the sliding surface's derivative. The STA algorithm drives both the sliding function and its derivative to zero in finite time without requiring the sliding surface's derivative. The sign (σ) function has a continuous structure since it is hidden under the integral. The chattering effect is decreased as a result of this process. SOSMC methods based on large-signal analysis are more efficient for DC/DC converters that supply CPL [33]. A buck converter STA-based SMC that feeds CPL has been developed for this research.

The purpose of the developed controller in this study is to adjust the output voltage of the buck converter feeding CPL based on the desired power and reference output voltage. The controller's switching signal is calculated by the proper duty cycle and sent to the source converter's switch to provide constant power to the CPL. The output voltage error and its derivative can be defined as state variables:

$$x_1 = v_o - v_{ref} \quad (18)$$

$$x_2 = \dot{v}_o = \dot{x}_1 \quad (19)$$

where $\dot{x}_1$ denote the derivative of x_1 and v_{ref} is the reference output voltage. The voltage error (x_1) and rate of change of voltage error (x_2) dynamics can be expressed as:

$$\dot{x}_1 = x_2 \quad (20)$$

$$\dot{x}_2 = \frac{v_{in}}{LC}u - \frac{v_{ref}}{LC} - \frac{x_1}{LC} + \frac{P}{C}\frac{x_2}{(x_1+v_{ref})^2} \quad (21)$$

A sliding surface function for conventional sliding mode control can be expressed as

$$\sigma = \lambda x_1 + x_2 \quad (22)$$

where λ is a positive coefficient for sliding line (When the system's degree is two, it is also called line instead of the surface) The traditional control input can be written as:

$$u = \frac{1}{2}(1 - sign(\sigma)) \quad (23)$$

Direct application of this control law, on the other hand, causes the converter to chattering, which is undesirable in practice. Thus, to suppress the switching frequency with a hysteresis band in a suitable range around the sliding line, it can be used as follows:

$$u = \begin{cases} 0 \ when \ \sigma > h \\ 1 \ when \ \sigma < -h \end{cases} \quad (24)$$

The following existence condition must be satisfied to preserve the movement of the error variables on the sliding line [23]. Define a Lyapunov function (*V*) as follows:

$$V = \frac{1}{2}\sigma^2 \quad (25)$$

The proposed switching control rule should guarantee that the time derivative of *V* is always negative to ensure controller stability and convergence of the state trajectory to the sliding surface. That is, the following inequality must be satisfied:

$$\dot{V} = \sigma\dot{\sigma} < 0 \quad (26)$$

3. STA Based SMC Design

Fig. 7 depicts the overall control architecture of a buck converter feeding CPL. A sliding surface must first be determined for SMC. The proposed sliding surface function that was chosen is as follows:

$$\sigma = i_L v_o - i_{Lref} v_{ref} + k(v_o - v_{ref}) \quad (27)$$

$$\dot{\sigma} = \left(\frac{v_{in}}{L} u - \frac{v_o}{L}\right) v_o + i_L \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right) + k \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right) \quad (28)$$

$$\dot{\sigma} = \left(\frac{v_{in} v_o}{L} u - \frac{v_o^2}{L}\right) + (i_L + k) \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right) \quad (29)$$

The dynamic response speed is related to the surface function's *"k"* value. To properly capture the output, the reference should be set to the appropriate value. When the first derivative of the sliding surface equals zero and u_{eq} (equivalent control rule) is defined. $For\ \dot{\sigma} = 0, u_{eq}$:

$$u_{eq} = \frac{v_o}{v_{in}} - \left(\frac{i_L L}{v_{in} v_o} + kL\right) \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right) \quad (30)$$

SMC's control rule (u) is chosen as follows to ensure stability:

$$u = u_{eq} + u_{sw} \quad (31)$$

$$u_{sw} = -\rho sign(\sigma), \rho > 0 \quad (32)$$

There are several drawbacks, such as the fact that it is not continuous and that one cannot entirely prevent chattering. Instead of sign, other functions such as sat(x), tanh(x), etc. are utilized. However, they lead to an increase in steady-state error and a decrease in accuracy. So, novel control rule control technique based on the STA algorithm instead of the u_{sw} is described. The resulting STA control rule is as follows [32]:

$$u_{sta} = -\alpha |\sigma|^{0.5} sign(\sigma) + \omega \quad (33)$$

$$\dot{\omega} = -\beta sign(\sigma) \quad (34)$$

The resulting novel control rule is as follows:

$$u_n = u_{eq} + u_{sta} \quad (35)$$

Eqs. (29) and (30) indicate the control rule of STA. *"α"* and *"β"* parameters used in the STA control rule are effective in adjusting the dynamic speed and in setting the steady-state error respectively [34]. The Lyapunov function is chosen to prove that the suggestion control rule ensures stability. Equation (25) should be always satisfied by using the proposed control law (u_n). Then, the following two conditions can be derived by substituting Eqs. (29) and (35) and into Eq. (26).

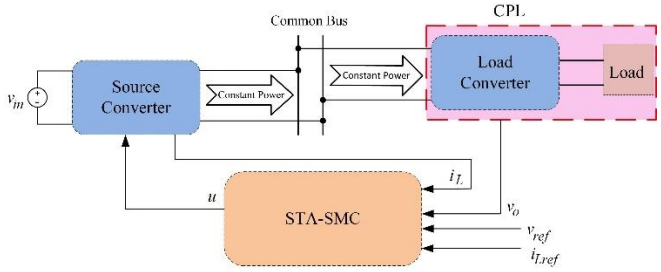

Fig. 7. General control schema of the buck converter feeding CPL

- If $\sigma > 0, u_n$ will be equal to 1, $\dot{\sigma}$ needs to be smaller than 0:

$$\dot{V} = \sigma \left[\left(\frac{v_{in} v_o}{L} u_n - \frac{v_o^2}{L}\right) + (i_L + k) \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right)\right] < 0 \quad (36)$$

$$\dot{V} = \sigma \left[\left(\frac{v_{in} v_o}{L} (u_{eq} + u_{sta}) - \frac{v_o^2}{L}\right) + (i_L + k) \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right)\right] < 0 \quad (37)$$

$$\dot{V} = \sigma \left[\frac{v_{in} v_o}{L} u_{sta}\right] < 0 \quad (38)$$

$$\dot{V} = \sigma \left[\frac{v_{in} v_o}{L} (-\alpha |\sigma|^{0.5} sign(\sigma) + \int -\beta sign(\sigma) dt)\right] < 0 \quad (39)$$

When α, and β are both greater than zero, stability is attained.

- If $\sigma < 0, u_n$ will be equal to $0, \dot{\sigma}$ needs to be greater than 0:

$$\dot{V} = \sigma \left[\left(\frac{v_{in} v_o}{L} u_n - \frac{v_o^2}{L}\right) + (i_L + k) \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right)\right] < 0 \quad (40)$$

$$\dot{V} = \sigma \left[\left(-\frac{v_o^2}{L}\right) + (i_L + k) \left(\frac{v_{in}}{C} - \frac{P}{C v_o}\right)\right] < 0 \quad (41)$$

If $k > 0$ and k is large enough, $\dot{\sigma}$ is greater than zero and stability is achieved.

4. Simulations and Experimental Results

To illustrate the performance of the proposed STA-based SMC, system which the DC/DC buck converter feeding CPL, has been tested by simulations and experiments. Simulations are carried out by Matlab/Simulink. Experimental results were obtained with hardware setup in the laboratory. The parameters of the system are offered in Table 1.

Table 1. Test rig parameters

Input Voltage (v_{in})	15-23 V
Reference Voltage (v_{ref})	10 V
Switching frequency (f_s)	20 kHz
Inductor (L)	340 µH
Capacitor (C)	100 µF
CPL Power (P)	5 W-20 W
α, β, k	5, 250, 5.10^3

4.1. STA-SMC Simulations Results

In Fig. 8, the states of the system and the sliding surface are shown without any disturbance. The sliding surface which error and its derivative are driven to zero is shown in Fig. 9. The output voltage response of the system to changes in the reference voltage is shown in Fig. 10. The output voltage successfully tracks its reference in all cases, as shown in Fig. 10. A reference voltage was captured in less than 1 ms. CPL current change is seen in Fig. 11. The constant power is obtained by adjusting the output voltage and current according to the reference. The change of error against the reference changes is driven to zero as seen in Fig. 12. The output voltage

responses according to the different initial conditions are shown in Fig. 13. The output voltage obtained by the STA-SMC has a faster start-up response than the output voltage obtained by the SMC.

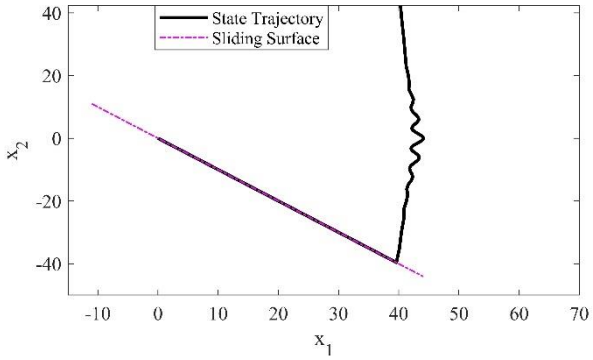

Fig. 8. State trajectories of the buck converter feeding CPL

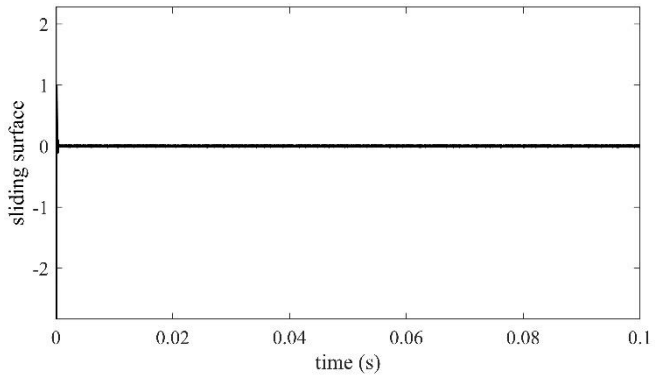

Fig. 9. Sliding function (σ)

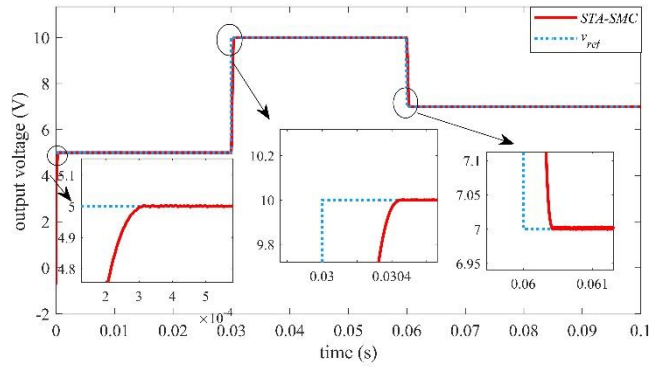

Fig. 10. The output voltage for STA-SMC

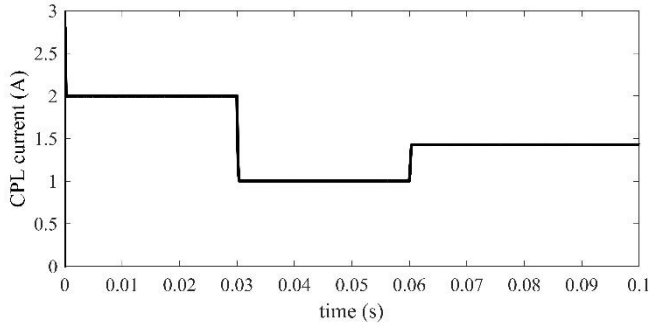

Fig. 11. CPL current for STA-SMC

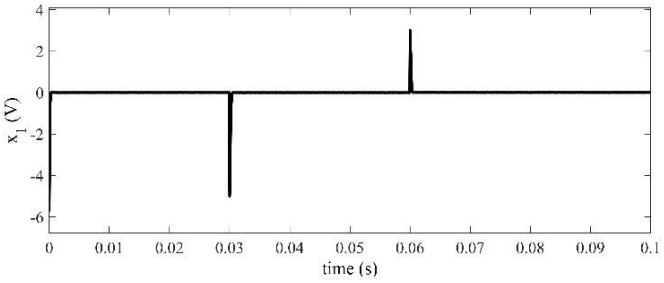

Fig. 12. Driving the error variable to zero

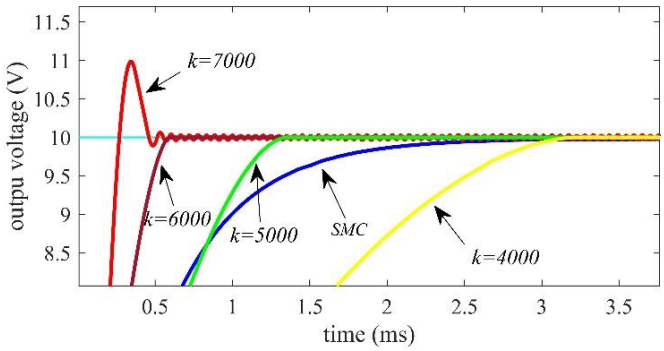

Fig. 13. Initial response of STA-SMC for different *k* values

4.2. Comparison with Conventional SMC

The dynamic performance of the suggested STA-SMC approach was also compared to conventional SMC using simulation results with step changes in the load power, input voltage, and reference output voltage. The response of the output voltage to step variations in the input voltage (v_{in}) is shown in Fig. 14 and Fig. 15. It is obvious from Figs. 14 and 15 that the output voltage follows its reference voltage more quickly and successfully. Furthermore, the step change in the input voltage has essentially no effect on the output voltage. However, in the SMC occurs the steady-state error.

The results presented in Fig. 16 and Fig. 17 show that the STA-SMC method is very robust against CPL power variations. The response of the output voltage to step variations in the reference voltage (v_{ref}) is shown in Fig. 18 and Fig. 19. It is obvious from Fig. 18 and Fig. 19 that the STA-SMC output voltage follows SMC faster. It is clear from the results presented with the proposed controller that the chattering is reduced.

Table 2 gives the settling time, tracking time, and steady-state error of the output voltage in controls methods. It can be seen that the STA-SMC outperforms all others in all cases. During CPL power and reference voltage changes, the proposed controller is catched the reference faster. The steady-state error of the proposed controller is very, very small for input voltage changes. But there is also the conventional SMC.

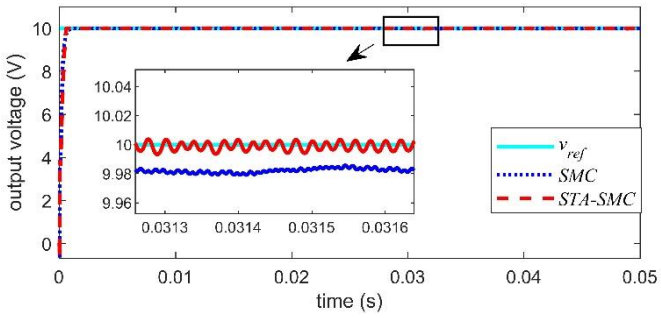

Fig. 14. The responses of the output voltage for step changes in the v_{in} from 20 V to 15 V

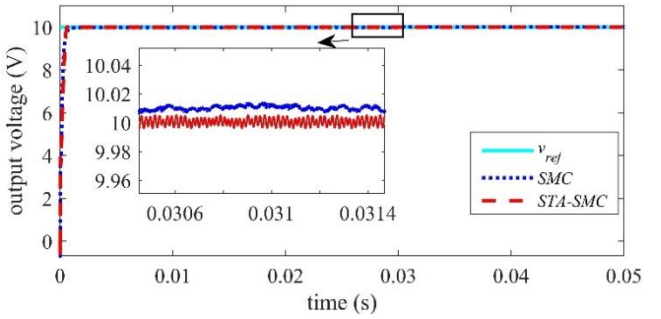

Fig. 15. The responses of the output voltage for step changes in the v_{in} from 15 V to 18 V

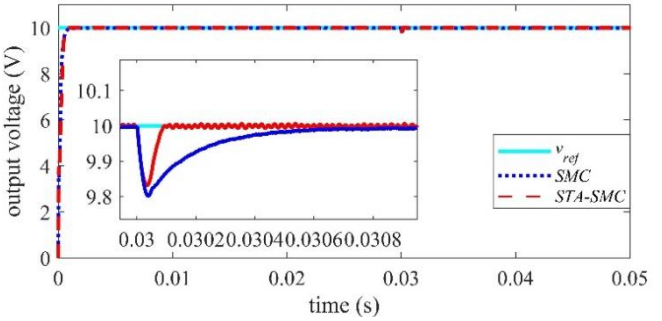

Fig. 16. The responses of the output voltage for step changes in the *P* from 10 W to 15 W

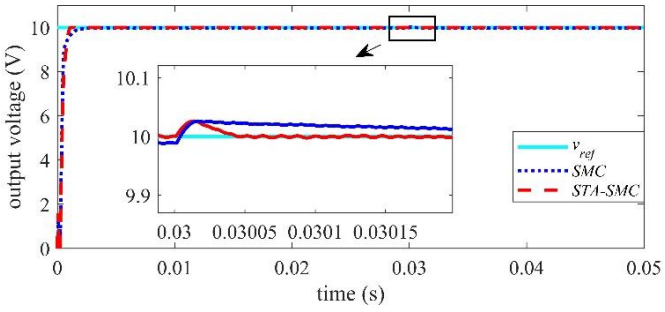

Fig. 17. The responses of the output voltage for step changes in the *P* from 15 W to 8 W

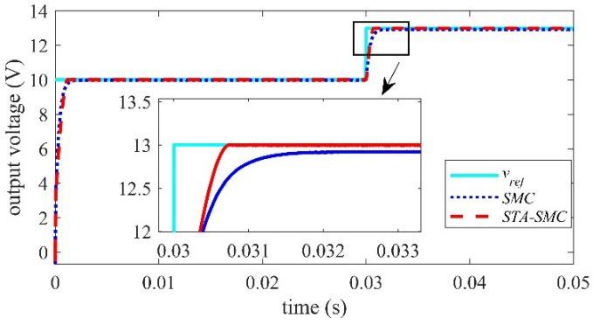

Fig. 18. The responses of the output voltage for step changes in the v_{ref} from 10 V to 13 V

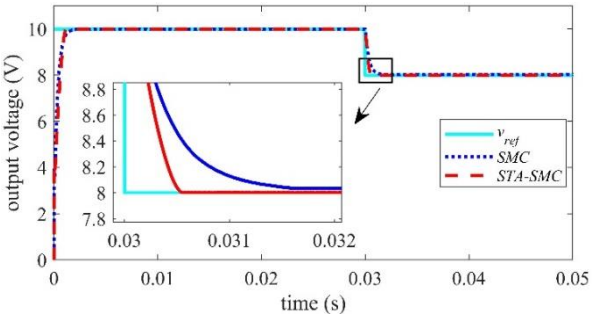

Fig. 19. The responses of the output voltage for step changes in the v_{ref} from 13 V to 8 V

Table 2. Dynamics responses for STA-SMC and SMC

	STEP CHANGES	STA-SMC	SMC
Settling time (ms)	from 10 W to 15 W	0.05	0.05
	from 15 W to 8 W	0.6	0.6
Tracking time (ms)	from 5 V to 10 V	0.06	10
	from 10 V to 7 V	0.06	10
Steady-state error (%)	from 10 W to 15 W	0.05	0.6
	from 15 W to 8 W	0.05	0.6

4.3. Experimental Results

In the MATLAB real-time environment, the controller was implemented. A DSPACE1104 was used to connect the buck converter circuit to the computer, with a PWM digital output supplying as the control signal. The TLP250's switching leads were connected to the DSPACE1104's digital input-output channel. In the buck converter, IGBT (2MBI75U4A) to drive were used TLP250. ET5410 DC load was modeled as CPL. The hardware setup is shown in Fig. 20.

The dynamic performance of the suggested STA-SMC was also tested using experimental results with step changes in the CPL power, input voltage, and reference output voltage. Fig. 21 shows the experimental response of the output voltage and CPL current produced using the STA-SMC approach for

a step-change in reference voltage (v_{ref}) from 5 V to 10 V. The output voltage takes about 3 ms to track its reference. The CPL current increases from 1 A to 2 A as a result of the change in the reference voltage. Fig. 22 illustrates the response of STA-SMC to the reference voltage change from 10 to 7 V. The output voltage takes about 3 ms to track its reference. To keep the constant power at 10 W, the CPL current is increased from 1 A to 1.4 A.

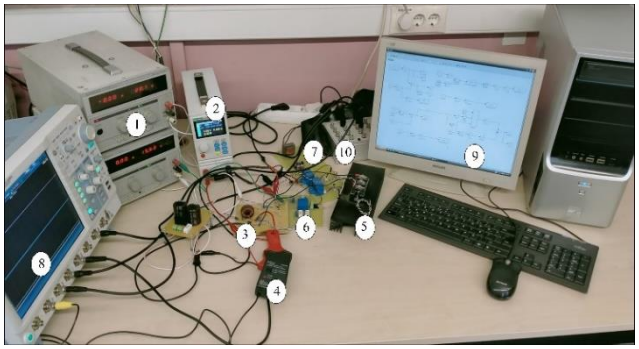

Fig. 20. Experimental setup (1) power supply (2) dc electronic load (3) buck converter (4) current probe (5) IGBT (6) voltage sensor (7) current sensor (8) oscilloscope (9) Matlab real-time environment (10) DSpace ADC-DAC, input-output

Because renewable energy sources can be employed in a DC microgrid, the buck converter's input voltage can be changed. Figs. 23 and 24 demonstrate the output voltage and control signal when the input voltage changes from 20 V to 15 V and from 15 V to 18 V. The output voltage follows the reference as 10 V. The STA-SMC adjusts the duty cycle rate of the switching signal to follow the reference voltage. Furthermore, as demonstrated in Figs. 23 and 24, the output voltage is unaffected by a step-change in the input voltage. When the input voltage is 20 V, the duty cycle ratio is approximately 0.51, and when the input voltage is 15 V, it is almost 0.67.

When the CPL power is changed from 10 W to 15 W and from 15 V to 8 W, the output voltage and CPL current are shown in Figs. 25 and 26. Experimentally obtained results demonstrate that the controller provides the desired power by adjusting the CPL current. Furthermore, the output voltage does not deteriorate because it follows the reference voltage. The small differences between simulations and experimental results are due to component tolerances and non-ideal influences in the practical system. The results presented in all Figs. show that the STA-SMC method is robust and fast against CPL power, the input, voltage and the reference voltage variations.

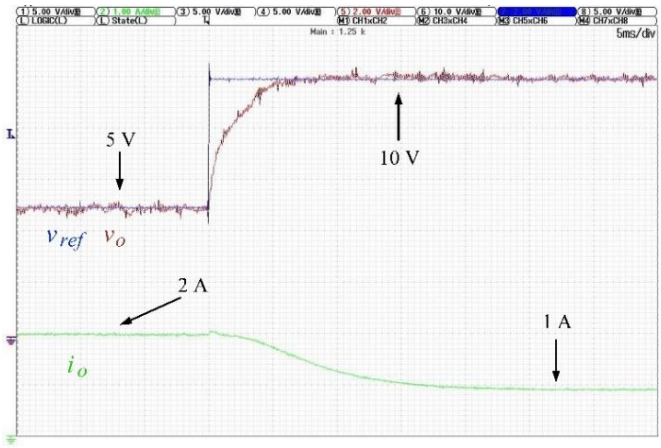

Fig. 21. Experimental responses of the output voltage and the CPL current for the step-change in v_{ref} from 5 V to 10 V

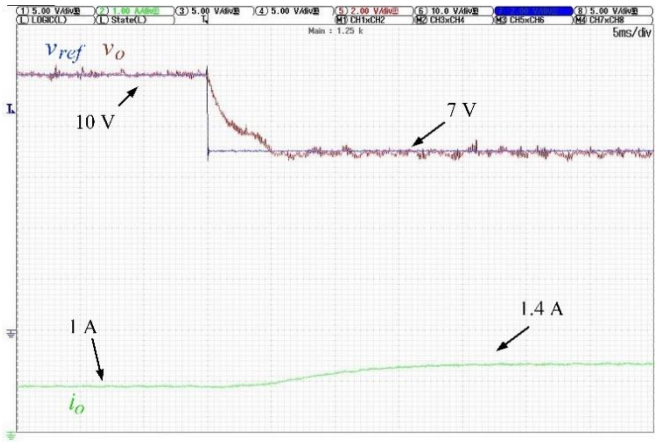

Fig. 22. Experimental responses of the output voltage and the CPL current for the step-change in v_{ref} from 10 V to 7 V

Fig. 23. Experimental responses of the output voltage and the CPL current for the step-change in v_{in} from 20 V to 15 V

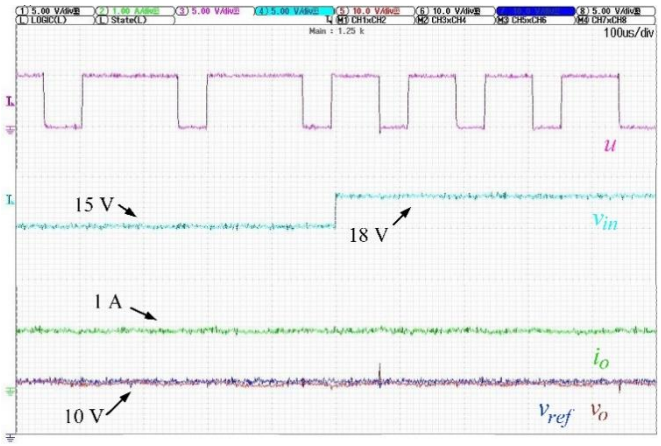

Fig. 24. Experimental responses of the output voltage and the CPL current for the step-change in v_{in} from 15 V to 18 V

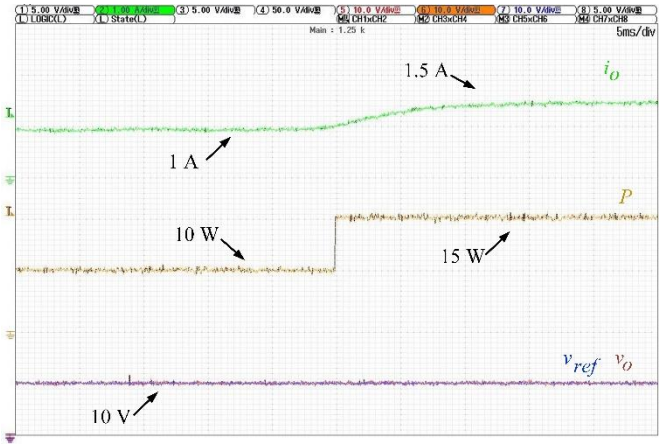

Fig. 25. Experimental responses of the output voltage and the CPL current for the step-change in *P* from 10 W to 15 W

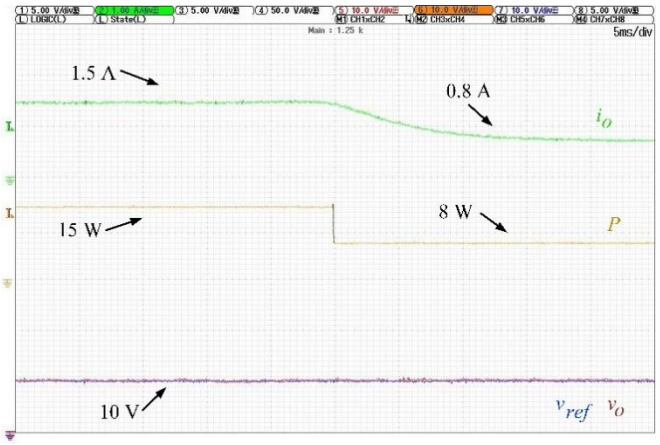

Fig. 26. Experimental responses of the output voltage and the CPL current for the step-change in P from 15 W to 8 W

5. Conclusion

In this paper, an STA-based SMC was proposed to solve the challenges of instability induced by the negative impedance impact of CPLs in the DC microgrid. The equivalent control approach was used in the proposed controller. By altering the traditional switching control rule, the proposed controller was added a super twisting algorithm (u_{sta}). The stability of the system was proved with the Lyapunov method. The suggested controller's superiority is in suppressing the high-frequency vibrations known as chattering, which is the primary drawback of traditional SMC. The accuracy of the controllers has been proven under different conditions which are input voltage variation, reference voltage variation, and CPL power variation, both the simulations in Matlab/Simulink and the experiments. Furthermore, the proposed controller was compared with the conventional SMC (or first-order sliding mode control). Simulation and experimental results depict that the STA-SMC is quite successful in obtaining very fast output voltage responses to disturbance.

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