# An Extensive Review on Fault Detection and Fault-tolerant Control of Multilevel Inverter with Applications

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**Abstract-** Multi-level inverters (MLI's) breakthrough in the current industrial market for various high power and high voltage applications mold the energy needs with renewable energy resources. Despite MLI's numerous advantages, their function is limited owing to heat and electrical stresses in power electronic components. In this study, a detailed state-of-the-art assessment of fault detection (FD) and fault tolerant control (FTC) systems is presented, along with the most recent developments and applications to assure the reliability of the multilevel inverter. A quick and accurate fault detection method necessitates a reliable and robust operation. This review systematically evaluates the various faults and further this study investigates the challenges associated with the switching scheme and harmonic control techniques of modulation methods for multilevel inverters. Further, this study envisioned the numerous fault detection methods available for MLI systems and addresses all the major types of faults and compares the several soft computing techniques with an emphasis on its diagnostic accuracy. Also, a comprehensive analysis of the different types of FTC methods based on the additional component requirement, challenges, and solutions are elaborated. The final part of this paper discusses the prospective future trends and research scopes on detecting and mitigating faults to enhance the reliability of the multilevel inverters.

**Keywords** Multilevel Inverter, Fault detection, Diagnostic accuracy, Fault tolerant control methods, Reliability, Renewable energy.

## 1. Introduction

Renewable energy sources (RES) have emerged as the most promising source of power generation during the last decade [1] due to rising global energy consumption. Notably, among all the renewable energy sources, solar and wind energy are the leading resources of electricity. Compared to wind energy, solar energy has notable features such as fast installation at a low cost, relatively silent operation, size, and maintenance [2]. By 2022, India intends to have 175GW of renewable energy capacity, comprising 100GW of solar power and 60GW of wind power [3]. Multilevel inverters (MLI) integrate smoothly with renewables such as solar, wind energy, and fuel cells as depicted in Fig.1. MLI coalesce between photovoltaic sources and the grid which is well suited for utility grid system applications with high voltage components. Using an array of power semiconductor devices, dc sources, and capacitors, the multilevel inverter generates a multiple-step voltage at the output [4].

The MLI can provide certain features such as improved waveform quality, a lower harmonic profile, less dv/dt stress on switches, a modular structure, and fault-tolerant operation [5]. Baker and Bannister invented MLI in 1975, which uses a series connection of full-bridge cells, each with an isolated dc supply and four switches is known as a Cascaded H-Bridge multilevel inverter (CHB) topology. Later, in 1981, Nabae and Akagi introduced a diode clamped or neutral point clamped (NPC) multilevel inverter topology, which divides the bus voltage into a set of voltage levels utilizing diodes and capacitors. Meynard and Foch proposed a flying capacitor (FC) multilevel inverter topology in 1992, a slight variation of the NPC MLI that uses clamping capacitors rather than clamping diodes [6]. These topologies are commonly referred to be multilevel inverter classical topologies as shown in Fig.2. MLI has a wide range of industrial and commercial applications, including power quality devices, electric vehicles, stand-alone or grid-connected solar systems, uninterruptible power supply, industrial drives, power transmission conveyors, MRI systems, and many more [7]. However, NPC MLI necessitate a large number of clamping diodes and capacitors; unbalanced voltage, uneven distribution of power loss, and the lack of modularity are the difficulties of NPC MLI at a higher level. Similarly, FC requires clamping capacitors, and charge unbalancing issues are the main limitations. Because of the constraints mentioned above, the NPC and FC topology is limited to a specific number of levels. The above difficulties can overcome by a cascaded h-bridge topology, which does not require any additional diodes or capacitors to provide an output voltage [8].

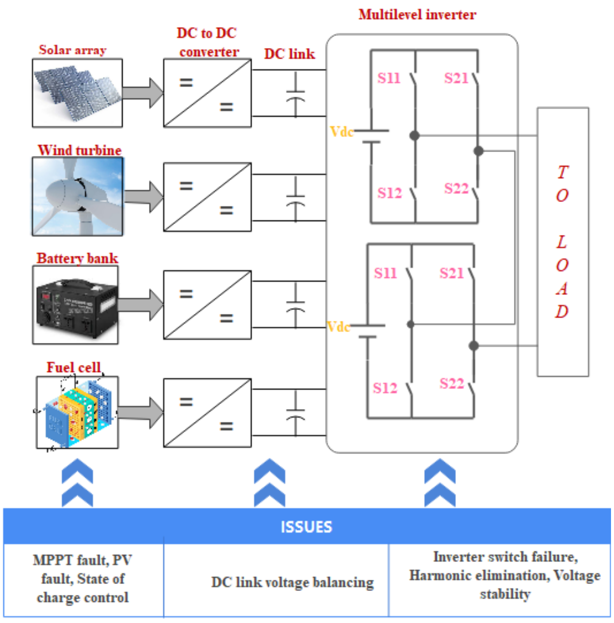



**Fig. 1.** Power conversion stage with RES

Furthermore, the number of voltage levels can be simply changed by adding or removing the h-bridge. It can also be characterized as symmetric or asymmetric topology based on the magnitude of the voltage source. In symmetric MLI, all sources have the same magnitude, whereas, in asymmetric MLI, all sources have unequal magnitudes. Because of the availability of independent dc sources in PV facilities, CHB MLI is best suited for large-scale systems of all MLI topologies. Compared to other topologies, CHB MLI is used at higher voltage levels since it has fewer components, a lower probability of switching failure, and easier switching control [9]. However, CHB limits with multiple independent power supplies of a higher number of voltage levels. The requirement of component count is a common problem in traditional MLIs; it is proportional to the output voltage levels. The larger number of components increases the system's complexity, control techniques, complexity in gate drive circuits, and failure rate of the components [10].

Based on the literature, about 21% of faults occur in power semiconductor switches. The two most common failures on MLI power switches are open circuit and short circuit failure. If an open-fault develops, the diode's body provides a freewheeling path. On the other hand, the short circuit fault is more challenging to resolve since it results in an excessive current that can cause significant damage to other components of the system [11]. Therefore, the MLI systems are susceptible to fault occurrences that severely impair the system's efficiency, reliability, and safety. Moreover, pulse width modulation (PWM) methods are used extensively in MLI systems to create switching pulses and minimize harmonics. Harmonics influence voltage fluctuation, losses, and power quality, which in turn impacts reliability [12]. Hence, it indicates the importance of fault detection (FD) and fault tolerant control (FTC) along with optimum modulation control technique to improve the reliability of the MLI systems. Fault tolerant control (FTC) is used to maintain the balanced output power to the load to ensure continuous operation. The function of FTC includes fault detection, determining the location and type of fault, and regaining its proper operation [13]. Few surveys on new FD and FTC techniques have been presented in [14]–[16]which provides the various methods and steps involved in fault detection and mitigation.

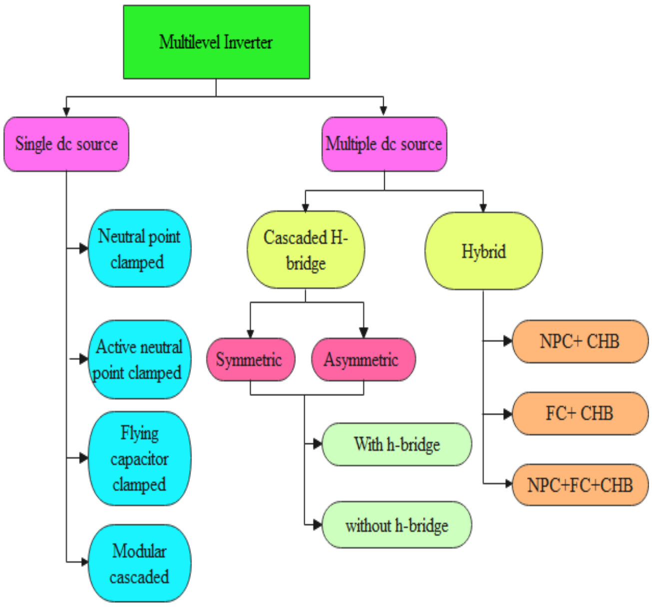



**Fig. 2.** Classification of Multilevel Inverter

As a result, detecting and mitigating faults while improving power quality is essential to achieving MLI system reliability. Hence, the originality of this review paper originates from its primary focus on emerging fault detection and fault tolerant control techniques of MLI topologies. Furthermore, a deep analysis was conducted to analyse numerous defects that occur in MLI systems, their impacts, protection issues, and the limits of standard protection mechanisms.

The rest of this article is structured as follows: Section 2 presents an investigation of the typical switch faults in a multilevel inverter. Section 3 discusses PWM approaches that use low switching frequencies (LSF) and high switching frequencies (HSF). Section 4 illustrates various methods of fault detecting and diagnosing approaches. Section 5 includes fault tolerant control in the multilevel inverter. Section 6 provides the applications of the fault tolerant multilevel inverters. Section 7 addresses the summary and research gap followed by the conclusion.

## 2. Typical Faults in a Multilevel Inverter System

Fault in any form causes serious damage to the system affects its reliability, if it is not detected for a long time, it causes the whole system to shut down. Power electronic components are the paramount importance to the multilevel energy conversion process. Power switches are the most prone to failure due to electrical, thermal, and mechanical stress. According to the survey, 34% of failures occur in power electronic devices of which 21% of failure occurs in semiconductor switches and 13% in solder joints as shown in Fig.3. It is reported that around 38% of failures in variable speed ac drives are caused by power device breakdown [17].

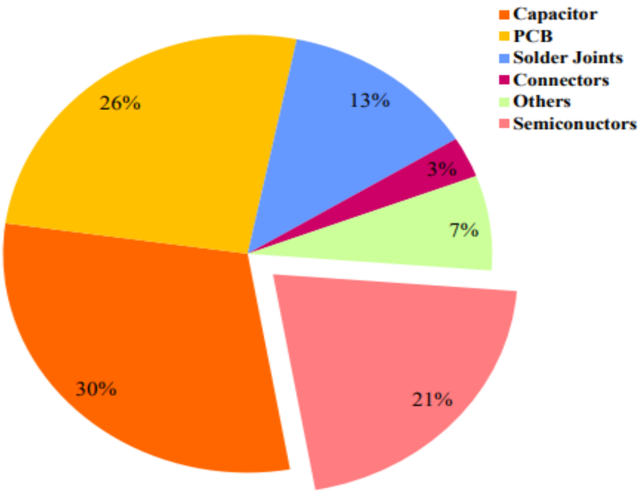



**Fig. 3.** Failure rate of power electronic components

In high power applications, multilevel inverter uses IGBT (Insulated Gate Bipolar Transistor) switches due to its high voltage and current ratings and short circuit current handling capacity. But the IGBT/ Power switches are subjected to failure due to voltage stress and temperature rise. Power switch electrical fault is characterized into two folds an open circuit (OC) and short circuit (SC) fault. Open circuit fault does not lead to a breakdown, the system can run at the reduced output voltage. The OC fault current flows the diode's freewheeling path. Short circuit fault current is difficult to handle because it produces abnormal overcurrent causes severe damage to the system [18]. Failure of protection device due to SC results in defective switch body diode becomes inaccessible. However, both faults should be recognized promptly before affecting the system's performance. Module failure occurs when several single switches fail in a single module due to OC or SC fault. It is an uncommon occurrence in the MLI system. The configuration of all possible switch faults in the multilevel inverter is classified as shown in Fig.4. Generally, the fault in the system causes a drop in output voltage, current, or both. The change in output voltage is determined as,

$$\Delta V_0 = V_{o\,ref} - V_{o\,act} \quad (1)$$

where $V_{o\,ref}$ is desired voltage, $V_{o\,act}$ is the actual voltage

This section gives insight into the various switch faults that occur in MLI, their effects, and the prerequisite of fault detection.

### *2.1.1 Open Circuit Fault*

An open circuit fault is a type of electrical fault that causes a broken path for an electrical current. Gate drive fault, damaging of inner wires in IGBT module due to thermal cycling, and a glimpse of the short circuit are the causes of OCF. In comparison to a short-circuit problem, an open-circuit defect does not cause significant damage but degrades the system performance. It results in current distortion (DC offset) and, through induced noise and vibrations, can cause secondary problems in other components [19]. In addition, an OCF can increase the harmonic content of the terminal voltage or current, which might affect the inverter-supplied equipment, such as transformers or electric motors, in the long run. Fig.5 shows single and multiple switches open circuit faults in a 3level inverter. The OCF and SCF are further classified into single switch fault (SSF) occurs either upper or lower switches and multiple switch fault (MSF) on the same leg or different leg.

Gate drive failure, electrical and thermal stress are the most common causes of SSF [20]. When the upper switch fails, the positive level in the output gets reduced likewise lower switch fails causes a reduction in negative output voltage. However, in MLI the top and lowest levels have just one switching state and another level contains more than one switching state (redundant switching state). If there is a loss at an intermediate level, the substitute state can be employed to create a similar output voltage. This is the reason that the exterior switches have a larger failure rate than the inner switch, and the rating of these switches must be chosen that to withstand the highest blocking voltage. Thus, the voltage stress on the upper switch gets increases, increasing its failure rate [21].

If a single switch fails, the other switches are more stressed to compensate for the missing voltage level, which could result in other switches failing at the same time. One or more switches fail at the same time known as multiple switch fault. Compared to SSF, MSF on the same leg is the serious fault condition which nullifies the output voltage leads to the whole system shutdown. Since the faulty level voltage cannot be compensated by a redundant switching state, a proper additional hardware setup may be required to clear MSF [22].

### *2.1.2 Short Circuit Fault*

A short circuit current that flows through the low resistance path leads to a rise in abnormal overcurrent than the nominal current. Overcurrent is caused by insulation damage, aging of wire, loose wire connection makes the live wire touches with neutral wire causing fault current within millisecond be thousands of times larger than the average operating current [11]. Excessive overcurrent, overvoltage, incorrect gate voltage, temperature rise causes the SCF. SCF is difficult to control since the current rapidly increases within a few seconds, causing extreme system damage. Standard protection systems such as fuses, relays, and circuit breakers can detect SCF, but not OCF. Fig.6 shows the short circuit fault under various conditions.

*2.2 Overvoltage and Undervoltage*

A phenomenon known as an overvoltage occurs when the magnitude of the voltage increases. When the voltage exceeds the normal voltage by 10% for more than one minute, an overvoltage condition exists. Undervoltage is caused by a dip in the voltage supplied by the power source during a transient. Undervoltage is commonly caused by a blown-out fuse, isolator, or contactor damage, an internal problem, or a low main voltage [23].

*2.3 Gate Drive Failure and Overheating*

Incorrect wire connection, low drive voltage rise, inverter malfunction, static electricity, and excessive gate wire length cause gate drive failure. When the gate drive fails, the inverter loses its unique voltage level; also, an inappropriate gate signal results in output distortion, such as an overvoltage or undervoltage condition [24]. SCF, overload, gate drive fault, and overcurrent cause device overheating. Overcurrent in the switches causes power loss and heat generation, which leads to overheating. The temperature at the junction causes inverter failure. To solve this issue, a precise thermal model with an over-temperature prevention device such as a temperature sensor should be implemented [25].

The conventional protection scheme such as fuse, circuit breaker, and protective relay is used for protecting the inverter in the event of a fault. When an OC fault occurs, a conventional protection device cuts the power from the dc source or gate drivers, consequently shutting down the entire operation and incurring significant production losses. Hence, these passive protective devices are ineffective when the system requires continuous operation and also place an added burden on other healthy switches.

*2.4 Impact of Faults on the Multilevel Inverter*

A multilevel inverter converts energy through a large number of switches. Semiconductor switch failure has a significant impact on the reliability of multilevel inverters. When an open circuit/short circuit occurs, the MLI deviates from its output voltage, causing the inverter to operate improperly. This can propagate downstream to the grid, resulting in future electrical failures. Additionally, it results in productivity loss and may result in an unexpected safety concern. If the failure persists for even a few seconds, it might have a detrimental influence on the load linked to it. Furthermore, the degree of switch failure varies according to topology and application. While an open circuit defect in CHB MLI causes one voltage level in a particular phase to be skipped, the other two phases continue to generate the same output voltage. Reduced voltage levels in drive applications do not affect the operation of the motor. However, in the case of grid-connected applications, this results in imbalanced voltage, which can eventually cause the entire system to shut down. Additionally, switch failures have a severe effect on the battery energy storage system.

Following an in-depth evaluation of numerous fault occurrences in multilevel inverters, an overall comparison of different fault and protection strategies is shown in the Table 1. Also, the following points are likely to be summarized;

- Among all the faults in MLI, open circuit and short circuit faults pose severe impacts and hence need to be detected and mitigated at first sight.
- Instead of the fault type, the amplitude of the fault current is influenced by the fault position in MLI.
- Conventional protection scheme fails to provide continuous operation when supplying critical loads.
- It is imperative to adopt an advanced tool for fault detection since standard methods cannot identify many defects and their locations.
- In addition to fault detection, fault identification is crucial for proper inverter isolation and maintenance.

## 3. Modulation Techniques

The modulation technique for the multilevel inverter is used to provide switching pulses through the gate circuit and to reduce the harmonics present in the output waveform. A modulation signal is intended to generate a stepped waveform that is the closest approximation possible to a subjective reference signal, containing amplitude and frequency fluctuations, as well as a fundamental component that is normally sinusoidal in a steady-state [26]. It is intended to regulate the output voltage/current as well as to calculate the primary parameters such as switching losses and percentage THD. The harmonics in the output waveform cause undesirable effects such as voltage fluctuation, improper operation, increased losses, and also it greatly affects the power quality. In MLI, many modulation approaches have been emphasized recently to overcome the aforementioned issues addressed in [27].

THD is the measured quantity of harmonics present in the waveform. The total harmonic distortion is defined “ratio of total harmonic content to the fundamental content in a waveform”.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n\_rms}^2}}{V_{01}} \tag{2}$$

$V_{n\_rms}$ is the rms voltage of $n^{th}$ order harmonics, $V_{o1}$ is the rms voltage of fundamental frequency. Several modulation techniques are classified as shown in Fig.7.

*3.1 Low Switching Frequency*

PWM techniques for MLI are categorized widely as fundamental/low switching frequency (LSF) modulation and high switching frequency (HSF) modulation. The switching frequency of the inverter is defined as the rate at which the switching devices are turned on and off. The LSF approach is one in which a switch commutates once or twice each cycle, whereas the HSF technique commutates multiple times per cycle [28]. A comparison of the LSF modulation scheme for MLI is elucidated in Table 2.

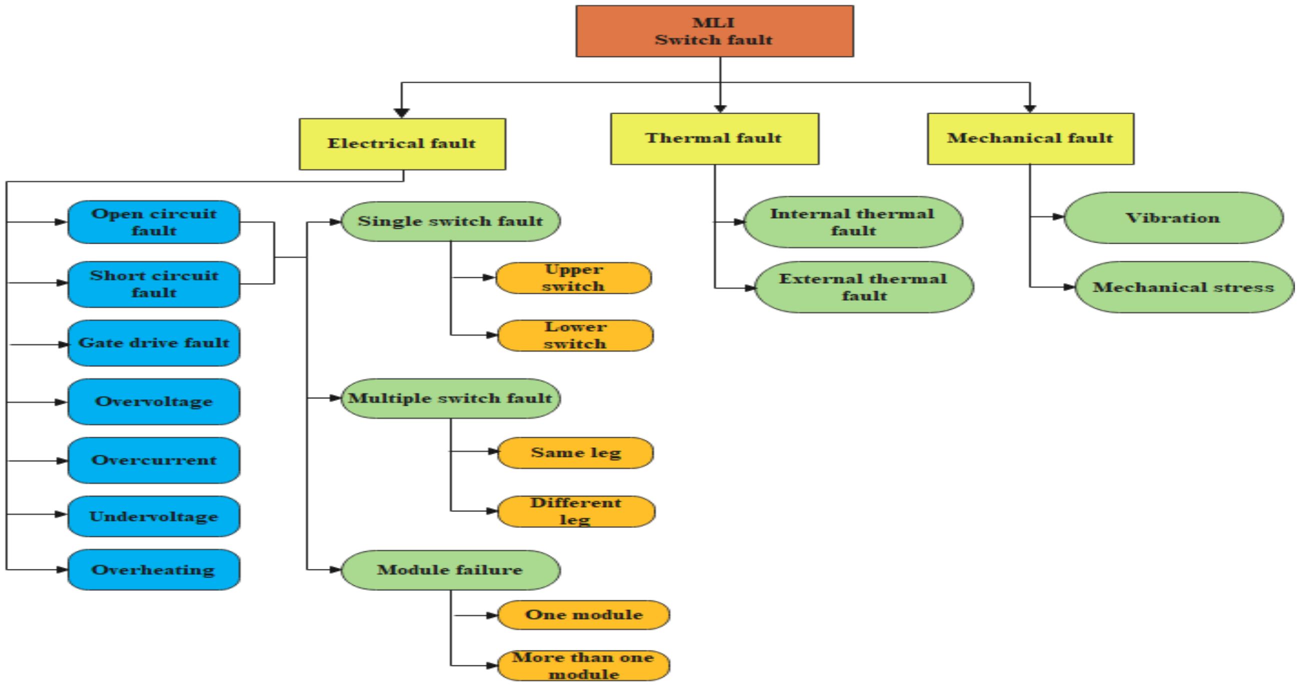



**Fig. 4.** Various faults in multilevel inverter

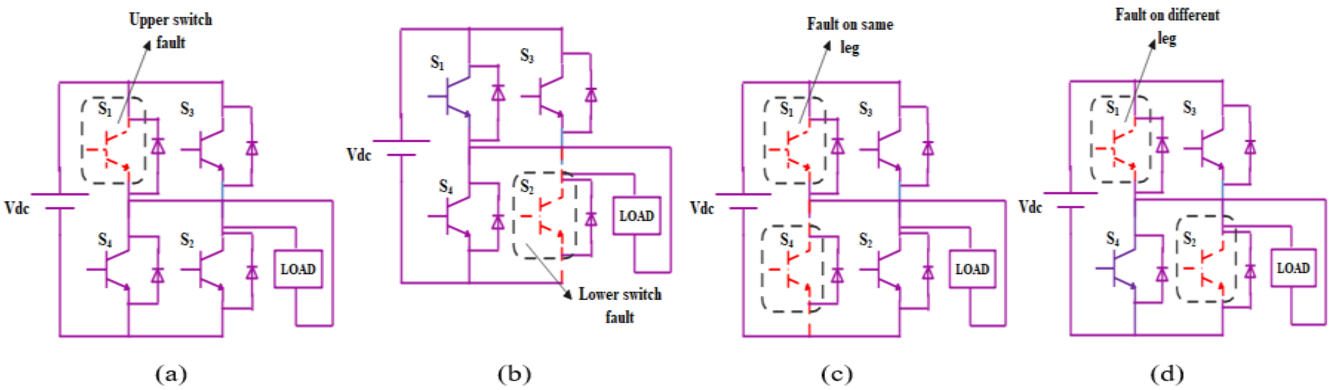



**Fig. 5.** Open circuit fault (a) SSF-U, (b)SSF-L, (c)MSF-same leg, (d)MSF-different leg.

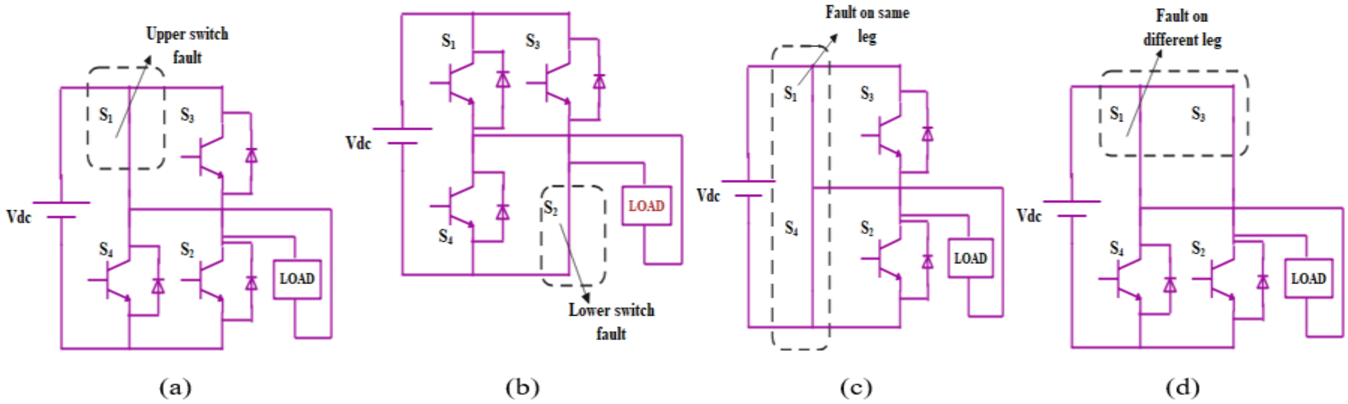



**Fig. 6.** Short circuit fault (a) SSF-U, (b)SSF-L, (c)MSF-same leg, (d)MSF-different leg

**Table 1.** Comparative detail of different types of faults and its protection methods

| S No | Fault | Significance | Event | Causes | Consequences | Protection methods |
|---|---|---|---|---|---|---|
| **1** | Open circuit fault | Very high | Common | Gate drive fault, damaging of inner wires. | The reduced output voltage, surge current, increased harmonic content, voltage stress. | Circuit breaker, relay. |
| **2** | Short circuit fault | Very high | Common | Overvoltage, loose wire connection, temperature rise, secondary breakdown. | The increased load current, Abnormal overcurrent, leads to other parts of the system to breakdown. | Protective relay, circuit breaker, fuses. |
| **3** | Gate drive failure | High | Common | Low voltage to drive, Improper connection | The reduced output voltage, surge current, lead to OC fault | Not available |
| **4** | Overvoltage | Low | Rare | Blown out fuse, contactor damage. | The unbalanced output voltage, lead to OC fault. | Relay, circuit breaker. |
| **5** | Overcurrent | Low | Rare | Improper control actions, unexpected load. | Distorted output, Damage to load. | Fuse, over current relay, solid-state circuit breakers. |
| **6** | Undervoltage | Low | Rare | Blown out fuse, contactor damage. | The unbalanced output voltage, damage to the load. | Circuit breaker, relay. |
| **7** | Over heating | Low | Common | Overcurrent, temperature rise. | Increases junction temperature, power loss. | Temperature sensors |

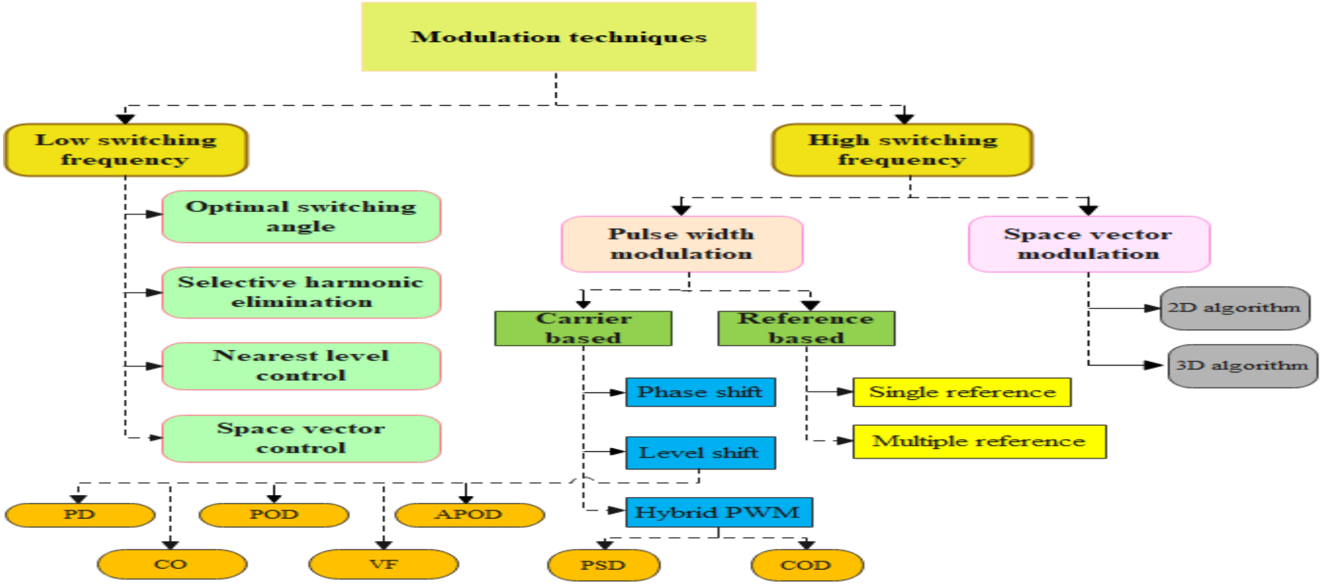
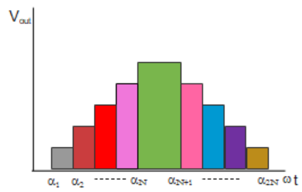
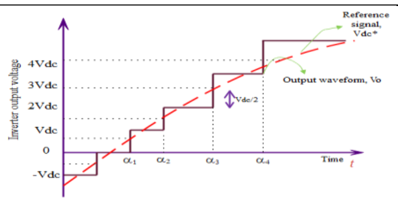
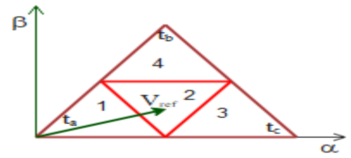



**Fig. 7.** Classification of pulse width modulation techniques

**Table 2.** Comparison of low switching frequency modulation technique for multilevel inverter

| Methods/ Parameters | Selective Harmonic Elimination | Nearest Level Control | Space Vector Control |
|---|---|---|---|
| Switching Scheme |  |  |  |
| Switching angle | $\cos(5\alpha_1) + \cos(5\alpha_2) + \cdots.\cos(5\alpha_s) = 0$ | $\alpha_{i+1} = \sin^{-1}\left[\frac{m_n + i}{(N-1)/2}\right]$ | Switching sequence based on vector combinations, $x^n$ |
| Techniques | Based on iterative and optimization techniques | Based on the reference voltage level | Based on reference voltage vector |
| Control complexity | Complex | Simple | Complex |
| Harmonic reduction | Elimination of specific lower order harmonics | Slight increase in THD | Low THD |
| Modulation Index | Limited to the modulation index | Wide range of modulation index | Limited to the modulation index |
| Benefits | • Well suited for the elimination of lower order harmonics<br>• Low switching losses<br>• Very low THD level<br>• Good steady-state response<br>• High efficiency | • Easy to implement in a closed-loop system<br>• Less computational time<br>• Eliminate the use of carrier wave<br>• High quality output | • Effective use of available dc bus voltage<br>• Significant reduction in THD and ripples in the output voltage<br>• Improved power factor<br>• Online based switching sequence easier to implement |
| Limitations | • Hard to solve offline-based mathematical equations for higher levels.<br>• Poor dynamic response<br>• Difficult to implement optimization techniques | • Not suitable for lower power applications levels results in low-quality output<br>• Unsuited for low modulation index<br>• Inappropriate for the elimination of specific order harmonics | • Hard to locate the nearest vector<br>• Limited to the number of voltage levels |

| | | | |
|---|---|---|---|
| | • Requires more computational time<br>• Inappropriate for low power applications require large capacitors | • Harmonic reduction is not effective<br>• Dynamic performance is not competent | • Predominant lower order harmonics cannot be eliminated<br>• The complexity of implementation increases with higher levels<br>• Implementation of overmodulation is complex. |
| Applications | • Ideal for high power application<br>• High power converters, Modular multilevel converter | | |
| Reference | [29]–[31] | [32]–[34] | [35] |

**Table 3.** Comparative detail of different switching angle calculation methods

| **Methods of calculating switching angle** | **Switching angle $\alpha_j$ for j=1,2…. (n-1)/2** | **Nature of α** | **%THD** | **Applications** |
|---|---|---|---|---|
| Equal phase | $\alpha_j = j\left({180°}/{n}\right)$ | Very small | High | Ideal for an inverter with smaller output voltage levels. |
| Half equal phase | $\alpha_j = j\left({180°}/{n+1}\right)$ | Small | High | |
| Half-height | $\alpha_j = \sin^{-1}\left(\frac{2j-1}{n-1}\right)$ | Wide | Medium | Ideal for an inverter with smaller and medium output voltage levels. |
| Feed forward | $\alpha_j = \left(\frac{\sin^{-1}\left(\frac{2j-1}{n-1}\right)}{2}\right)$ | Very wide | Low | Most suited method for any level of output. |

*3.1.1 Optimal Switching Angle*

The harmonic reduction is achieved by selecting the optimum switching angle. Thus, the calculation of the switching angle is critical to improving the output quality of the waveform produced. The switching angle (α) for different modulation indexes is calculated using

$$\alpha_j = \sin^{-1}\left(\frac{\pi}{4}\frac{(j-\frac{1}{2})}{n}\right) \tag{3}$$

Where $\alpha_j$ is the j[th] switching angle of different modulation index '$n$'

The switching angle in the first quadrant period is known as the main switching angle. i.e (0-90˚). From the main switching angle, it is possible to compute the switching angles relating to the second, third, and fourth quadrants, i.e., from (90˚ to 360˚) [36]. Table 3 presents a comparative detail of four ways of calculating the switching angle.

*3.1.2 Selective Harmonic Elimination (SHE)*

The selective harmonic elimination technique is widely used in MLI due to direct control over lower harmonic order and dc source utilization. Non-linear transcendental SHE equations can be used to compute the switching angle [37]–[39]. By estimating the switching angle, the SHE technique attempts to suppress lower-order harmonics within the allowed range. When solving SHE equations, the unknown switching angle $\alpha_1, \alpha_2 \cdots \alpha_n$ is obtained which must satisfy the condition $0<\alpha_1<\alpha_2<\ldots\alpha_n<\pi/2$. The Fourier series expansion to find output voltage and odd harmonic component will be written as,

Output phase voltage, $V_{(\omega t)} = \sum_{n=1,3,}^{\infty} V_h \sin(n\omega t)$ (4)

Odd harmonic component, $V_h = \frac{4V_{dc}}{h\pi \sum_{i=1}^{m}\cos(h\alpha_i)}$ (5)

where h is the number of odd harmonics and $\alpha_i$ is the switching angle. This technique offers high-quality output and elimination of lower-order harmonics maintaining the switching frequency at minimum level [40] and preserving fundamental components. However, solving nonlinear SHE equations is a significant challenge in achieving switching angles. To address this issue, several solutions have been proposed, which are broadly classified into two categories: numerical and algorithm-based methods as shown in Fig.8. Iterative numerical methods, such as the Newton-Raphson method, are used to solve the equations at the beginning of the process [41]. However, larger switching angles and large voltage levels are not reliable using this method. Using trigonometric identities, nonlinear transcendental equations are transformed to a set of polynomial equations in the resultant theory technique [37].

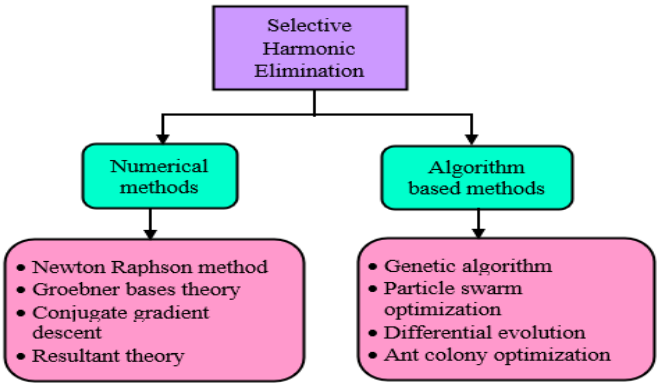



**Fig. 8.** Different types of SHE techniques

Select the first unknown identity values and then apply them in the same equation to get the set for waveform output of switching angles. The degree of polynomials grows with the number of DC sources, increasing the computing complexity of the resulting polynomials. Also, the number of harmonic eliminations is large. Groebner Bases Theory approach [42] is a recent development in SHE compared to previous techniques, it has no beginning value for iteration, all solutions are determined, and it finds the best switching angle with more accuracy. Moreover, the iterative approach requires beginning values, which are complex and time expensive. Thus, an evolutionary algorithm-based technique is devised to minimize SHE equations. Algorithms play a role in the development of the switching angle [43]. Algorithms are mostly used to optimize the harmonic profile and determine the switching angle. Over the recent years, numerous algorithms based harmonic reduction approaches have been developed [29]–[31], [38] such as Genetic algorithm, Particle swarm optimization, Ant colony optimization, Bee algorithm, Clonal search algorithm, Bacterial foraging algorithm, Differential evolution are used to eliminate the lower order harmonics and improve the harmonic spectrum. These approaches are efficient, provide the optimal switching angle, and can be applied to any number of levels [44]. While the SHE approaches eliminates harmonics, it has a few shortcomings, including the switching angle must be kept below $\pi/2$, a slower response time during transient situations and pre-defined computations are necessary. When solving transcendental equations numerically, the optimal switching angle may not be obtained, and the operation is also time-consuming. Further, to enhance its capability it needs some optimization techniques which can find the solution for the full range of modulation indexes [45]. However, this strategy is appropriate for low-level inverters but not for high-level inverters.

*3.1.3 Nearest Level Control (NLC) method*

NLC method is simple and accurate to find optimum switching angles for various modulation indexes. The nearest level is chosen by comparing the sinusoidal reference with the output voltage, a technique known as round modulation. NLC method is not involved to solve hard mathematical equations and is not needed to find the nearest vector as SHE and SVM methods both require more computational time as compared to NLC. NLC technique is suitable for higher voltage levels since for lower voltage levels the harmonic distortion is quite high [32]. The formula to find the nearest level is,

$$\text{Nearest voltage level} = x * round\left(\frac{s}{x}\right) \qquad (6)$$

where $x$ is an integer. This method directly calculates the switching signals and pulse duration of each phase and does not require a carrier triangle signal. This method is preferred over the other method due to lower switching losses and efficiency. A hybridized PWM technique is used in [46] to find the wider control range of output voltage. This system runs at frequencies ranging from 50 to 60 Hz and can be simply scaled up to N levels. Hence, NLC is not appropriate for lower modulation indexes, the total harmonic distortion (THD) is increased. In addition, this method does not eliminate a certain order of harmonics and does not accurately track the reference signal [34].

*3.1.4 Space Vector Control (SVC) Method*

The objective of this method is to find the vector that is closest to the reference vector and has the smallest space error or distance between them. Natural selection of the nearest vector may decrease commutation and switching losses. A different approach to finding the nearest vector to the reference vector in a sample period is discussed in [35].

*3.2 High Switching Frequency (HSF)*

HSF is further broadly classified as pulse width modulation (PWM) and space vector modulation (SVM) techniques. A comparison of the HSF modulation scheme for MLI is elucidated in Table 4.

*3.2.1 Pulse Width Modulation (PWM)*

The PWM technique is the most widely used modulation technique in the multilevel inverter. It is further classified into carrier-based PWM and reference-based PWM. The switching pulses generated using the PWM scheme give the switching instant of the inverter.

*3.2.1.1 Carrier-Based PWM (CPWM)*

Comparing the triangular carrier signal to a sinusoidal reference signal provides a pulse that governs the switching process of power electronic switches. This is referred to as carrier-based pulse width modulation (PWM). The number of available carrier signals in a system with N levels is N-1. Comparative study of PS & LS PWM method for 13 level MLI was addressed [47].

*A. Phase Shifted Carrier (PSC) Method*

In PSC PWM, all the carriers have the same peak amplitude and frequency but there is a phase shift between adjacent carriers. It requires an (N-1) triangular carrier signal for n voltage level. Phase shifted by an angle $\emptyset_{cr}$,

$$\emptyset_{cr} = {360°}/{n-1} \qquad (7)$$

For a 3-level inverter, the horizontal phase shift of 180˚ is required. It has a superior harmonic profile due to the lower switching frequency, which results in a lower dv/dt and less EMI. Thus, power handled by each module is evenly distributed and has more THD reduction compared to LSPWM. A simple and flexible PSC method is proposed in [48] for lowering common-mode voltage, switching frequency, and commutation losses in five-level CHB. The general concept of PSC PWM implementation is discussed in [49].

*B. Level Shifted (LS) Carrier Method*

The LS PWM is represented by (m-1) carriers in an adjacent vertical band. All the carrier wave has the same amplitude and frequency but is vertically displaced with each other [47]. The carriers in PD PWM are in phase above and below the reference plane [50]. In POD PWM, all of the carriers above the reference plane are out of phase with the carriers below the reference plane [51]. All of the carrier signals in the APOD approach are 180 degrees apart from one another [52]. The carrier overlapping (CO) approach involves the placement of (m-1) carrier is disposed of in such a way that the bands they occupy overlap each other; the overlapping vertical distance between each carrier $A_c/2$. The distance between neighboring carriers is half their amplitude. Because the reference intercepts the carrier more often than the PD technique, the CO approach reduces harmonic distortion on line voltage [53]. To compensate for the power loss in NPC inverters, variable frequency PD is most often used. The external switches commutate more often than the internal ones [54].

Variable frequency (VF) PWM is used for "m" level inverters. The carrier signal has the same amplitude and phase but varies in frequency. This strategy is utilized when the frequency of the upper and lower switches is greater than the frequency of the intermediate switches. LS-PWM provides a more accurate load voltage spectrum with less distortion than PS-PWM because the carrier waveforms are not phase-shifted relative to one another. The line-to-line voltage and harmonic spectrum for several PWM techniques such as PD, POD, APOD, IC, PSC, and VFC were examined in [55].

*C. Hybrid PWM (HPWM)*

It is the combination of low switching and high switching frequency PWM. The primary objective is to reduce the inverter's losses by lowering the switching frequency of the higher power units [33]. The hybridized technique is mainly used for CHB to maximize the controlling range of output voltage and to evaluate the optimum operating point.

*3.2.1.2 Reference-Based PWM*

Further subcategories of reference-based PWM include sinusoidal, trapezoidal, third harmonic injection, and discontinuous reference PWM. Sinusoidal PWM is widely known PWM approach that generates pulses for the inverter switches by comparing a sinusoidal reference wave to a triangular carrier wave. While sinusoidal PWM is simple to understand and implement, it is unable to fully utilize the DC bus supply voltage available [56]. To use the better dc voltage, a third harmonic component is injected into the reference voltage. Compared to SVM, THIPWM provides the lowest common-mode voltage.

Third harmonic injection PWM (THI-PWM): For improving the harmonic characteristics of output current and to utilize dc voltage effectively, a third harmonic offset voltage is injected into the reference waveform. In [57], the third harmonic component is injected into the sinusoidal reference signal to increase the fundamental component to 15%. Comparatively the output voltage produced by pure sinusoidal reference is increased by 15% using the third harmonic component. However, the output voltage contains a third harmonic component. The third harmonic injected PWM signal. The alternating carrier polarity (ACP) based third harmonic injection sinusoidal PWM is proposed in [58] to utilize the dc bus voltage utilization compared with SVM.

*3.2.2 Space Vector Modulation (SVM)*

SVM is a digital modulation method that creates a switching sequence based on vector representation. A vector representation is used to regulate the switching pattern of the switches. To illustrate the magnitudes and phases of each vector, the vectors are arranged in a hexagonal pattern. The standard method that represents the SVM in the α-β frame is called the α-β SVM. The reference voltage can be determined using the formula [35],

$$V_{ref} = {}^{2}/_{3}\,(V_a + \alpha V_b + \alpha^2 V_c) \qquad (8)$$

Where $\alpha = e^{j2\pi/3}$. The switching state can be calculated using $m^n$, where m is the number of levels and n is the number of phases. For 2 level SVM, there are $m^n = 2^3 = 8$ switching states. For 3 level SVM, there are $m^n = 3^3 = 27$ switching states. The axis of α and β is along 0˚ and 90˚. Six active vectors and two zero vectors are contained in a two-level inverter, while a three-level inverter contains 24 active vectors and three zero vectors. Fig.9 shows the SVM for the 3L inverter [55].

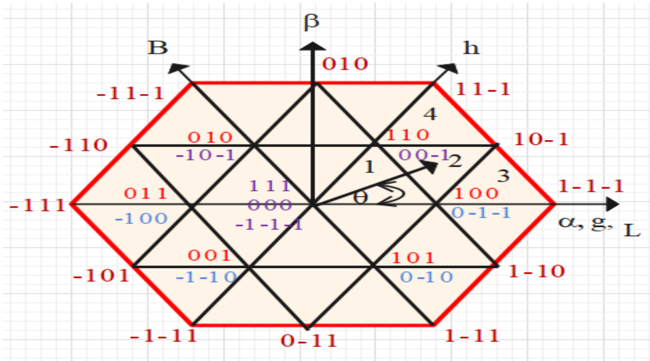



**Fig. 9.** Three-level SVM

At the constant voltage and constant frequency, the reference voltage vector $V_{ref}$ revolves at angular frequency 'ω' around the origin of the space vector diagram. If the reference vector is positioned in-plane I, the closest vectors are $V_1$ and

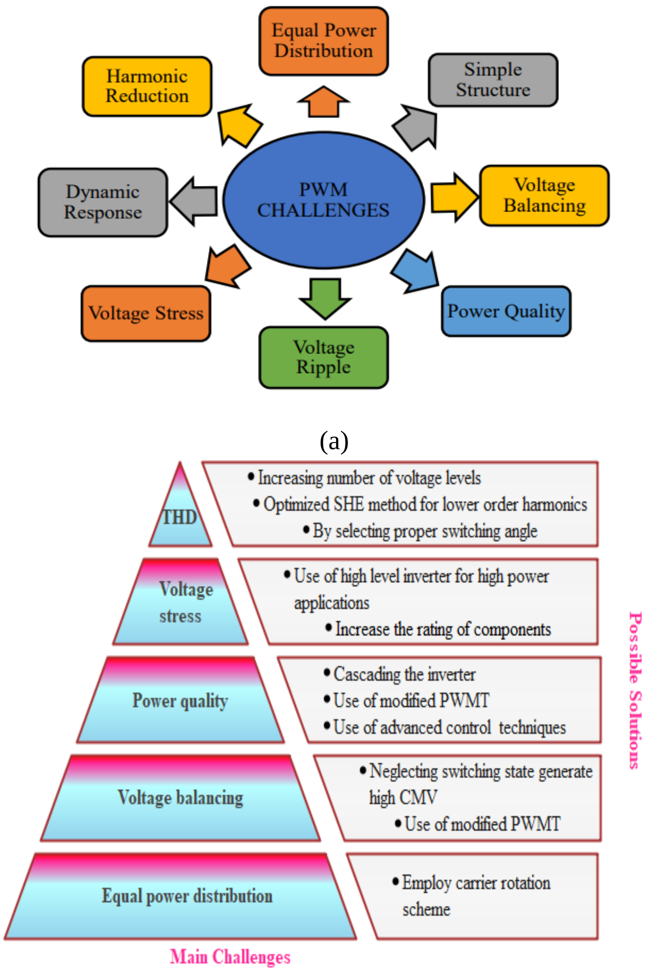
$V_2$, whereas $V_z$ is the zero vector. In a typical SVM, dwell durations are computed as the number of switching states and triangles develops. As a result, the conventional SVM technique is more complex to implement and consumes more computing time. The reference vector is found using the Nearest Three Vector (NTV) approach [59]. This method is effectively used for balancing the dc-link in the NPC inverter.

Reduced common-mode voltage (CMV) can be easily achieved by excluding switching states that generate significant CMV. The coordinate transformation method is used to calculate the position and duty cycle of a given reference vector. This necessitates the use of a lookup table to store the switching sequence [60]. Since this modulation technique is employed in three-level inverters designed for greater power applications. Nonetheless, as the system becomes more complicated, the SVM technique is limited to a greater number of voltage levels. As a result, the maximum number of levels is limited to five.

*3.3 Challenges Involved in PWM Techniques*

MLIs confront several issues when it comes to modulation and control systems. The issues namely voltage balancing, harmonics, power quality, dynamic response switching loss, and even distribution of power are all concerns with the PWM approach. These challenges create significant impacts on the output of MLI that affect the system's reliability and efficiency. To overcome these issues, and MLI with precise modulation and control scheme should be implemented [61]. From recent research, it is inferred that reducing THD and overall loss has a significant effect on MLI performance.

The challenges faced by modulation technique and possible solutions are depicted in Fig.10. Foremost, harmonics is the major challenge because it directly affects the inverter power quality. To eradicate harmonics, the first approach is to use various PWM switching strategies such as sinusoidal PWM [62], space vector PWM [55], SHE-PSO optimization [63] to suppress harmonics. Multicarrier PWM like PD, POD, APOD PWM techniques are fruitful for eliminating harmonics, among PD PWM found a significant harmonic profile than others.




(a)

(b)

**Fig. 10.** Challenges and solutions involved in PWM (a) Challenges, (b) Possible solutions

However, carrier-based methods are effective on low amplitude harmonics but not suitable for high amplitude harmonics. Nevertheless, these methods are not capable of eliminating lower-order harmonics. The lower order harmonics as $5^{th}$, $7^{th}$, and $9^{th}$ are suppressed using the selective harmonic elimination (SHE) method [31], [40]. The hybridized PWM technique proposed in [64] utilizes the NLC and SHE method for a wider range of output voltage control. In this method, the NLC technique alone reduces harmonics up to 5.37%. Increasing the number of voltage levels can also help to minimize THD.

Likewise, the issues associated with unequal h-bridge usage in LS-PWM can be resolved by rotating the switching sequence. However, while phase shift PWM distributes power evenly throughout modules, the unbalanced dc-link voltage raises voltage stress between components, which may be avoided by altering the PWM approach. According to the literature, both LSF and HSF approaches have their benefits and drawbacks. Thus, by adopting the appropriate control technique for the MLI topology, the difficulties may be alleviated

## 4. Fault Detection Methods in Multilevel Inverter

Fault detection and isolation (FDI) is important in MLI before implementing reconfiguration technique and it is defined as "a monitoring system used to detect and diagnose flaws in a system". FDI has been characterized into fault detection (FD) and fault isolation techniques. FD ascertains the occurrence of fault and fault isolation affirms the type and location of a fault. Fault identification gives the magnitude of the fault. Generally, the FD approach efficiently utilizes output voltage or current data to identify inverter faults [65]. The reliable FD technique should have the following features:

- Capability for multiple fault detection without affecting the power quality.
- It must be simple, reliable, and cost-effective.
- It should have competence for locating and distinguishing faults.
- It should be quick and precise in detecting multiple faults and suitable for non-linear systems.
- It should be suitable for FTC and applicable to any type of MLI topologies.

Therefore, this section critically evaluates the performance of many new fault diagnostic approaches based on the approaches. A few online fault detection systems have evolved recently in response to the increasing demand for reliable fault detection techniques. Hence, the majority of open-circuit fault detection approaches rely on algorithmic techniques, whereas short circuit fault detection depends on hardware methods. For a clear understanding, steps involved in the general fault diagnosis approach are shown in Fig.11 and the various fault detection methods are depicted in Fig.12. The fault detection methods are categorized into model-based, data-based, and signal processing techniques. In the subsections, each technique is thoroughly examined, and a summary of several research works in each area is also provided.

### *4.1 Model-Based Methods*

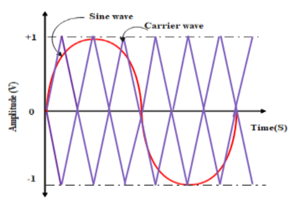
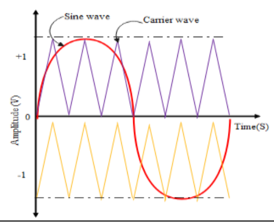
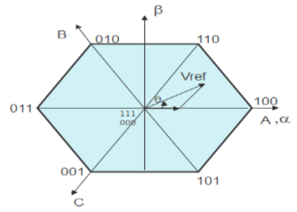
The model-based system makes use of analytical information about the system to detect faults. This method is based on comparing real-time parameters to the model-predicted values to detect system failure. When an inverter is under faulty condition, the output voltage or current signals will differ from the normal condition. These signals (residuals) are analyzed and compared to specified requirements to determine the occurrence and location of the fault [66]. The block diagram of the model-based FD method is presented in Fig.13. The model-based method is further classified into parity equations, state estimation and parameter estimation approaches. The state estimation approach for diagnosing open circuit fault by comparing the estimated and measured voltage has been proposed in [67]. For an electric vehicle, a model-based fault diagnostic technique was developed in [68] for OCFs by utilizing a sliding-mode observer to acquire an estimation of the phase current to generate a residual. Hence, it is an accurate method for fault diagnosis but increases mathematical complexity for the system. Primarily, the parameter estimation technique [69] establishes a threshold value; if the real-time parameters exceed the value, a fault has occurred; otherwise, the system is estimated as fault-free mode. However, the inverter's reliability is entirely dependent on the accuracy of the model parameters used to establish the parameter estimation method.

The voltage-based approaches have been presented [70], in which the terminal voltage is monitored and compared to the applied switching state, however, these methods necessitate the installation of extra voltage sensors, which raises the cost. The FD approach based on zero voltage switching and AC slope is proposed in [71]. However, this method is slow which needs three fundamental cycles to identify and isolate the faulty switch. Fast and online-based fault diagnosis for FC MLI presented in [72] uses PS PWM to detect the OC fault by using voltage and current data along with the switching signal. The system doesn’t require additional hardware setup or sensors.

In [73], the author suggested an open circuit fault diagnosis approach for generalized CHBMLI using PD PWM. This system provides bridge voltage information together with half-cycle mean voltage (HCMV) values are utilized to identify faults. Using a fault identifier, the fault can be identified within one cycle of output voltage, minimizing processing needs.

A method based on voltage magnitude is presented in [74] that detects the fault within a few 100 $\mu$s using phase-shifted PWM despite relatively slow and less accurate method. Fault identification and detection method for nested neutral point clamped (NNPC) MLI is introduced in [75] to locate OCF using voltage and current measurement values. The SC fault detection and isolation using only one voltage detector per phase is suggested [76], the location of the faulty switch is detected by comparing the finite number of observed voltage levels with fault signature sets. The model-based techniques are more accurate but utilizes additional voltage or current sensors which increases the cost of the system.

**Table 4.** Comparison of high switching frequency modulation technique for multilevel inverter

| **Methods/Parameters** | **Pulse width modulation** | | **Space vector modulation** |
|---|---|---|---|
| | **PS PWM** | **LS PWM** | |
| Switching Scheme |  |  |  |
| Techniques | Carrier-based technique | Carrier-based technique | Non-carrier-based method/ Switching sequence based on reference vector |
| Control complexity | Simple | Simple | Complex |
| Harmonic reduction | Improved harmonic reduction | Slightly increased THD compared to PS PWM | Lower harmonic content |
| Benefits | • Simple in structure<br>• It offers a low THD value<br>• Equal utilization of switch<br>• Even distribution of power and stress among the module<br>• Easy to implement.<br>• No need to rotate the switching pattern | • High quality output voltage waveform<br>• Suppress dc voltage ripples<br>• Appropriate for FC and CHB topology<br>• Easy to implement | • Eliminate the use of triangular carrier waves.<br>• Redundancy in switching state<br>• Lower common-mode voltage<br>• Suitable for FC and NPC topology<br>• Good dynamic response<br>• Provide better dc-link voltage balancing |
| Limitations | • Poor dynamic response<br>• Not suitable for a low-speed operating region of the motor | • Uneven distribution of losses<br>• Unequal voltage stress<br>• (N-1) carrier signal makes complex driver circuitry<br>• Rotation of switching pattern makes complexity in control | • Complex switching scheme<br>• Limited to the number of voltage levels<br>• Inappropriate for overmodulation |
| Applications | • Industrial drive applications<br>• Solar PV applications | | • Traction drive application<br>• Industrial applications |
| Reference | [47]–[49] | [50]–[55] | [59], [60] |

Although, model predictive control technique was developed to reduce the usage of additional sensors and minimize computational burden.

*4.1.1 Model Predictive Control Techniques*

Recently, the model predictive control (MPC) method is the most prevailing method of fault diagnosis in multilevel inverters. The MPC algorithm forecasts future states through its optimization process, which can be compared to the present state for fault detection without the requirement of additional sensors. MPC is an optimization technique were used to find out the optimal switching angle and it has a good steady-state and dynamic response of the system [77]. This method can directly control the load connected to the inverter and is most widely used in inverter topologies that require a large number of switches.

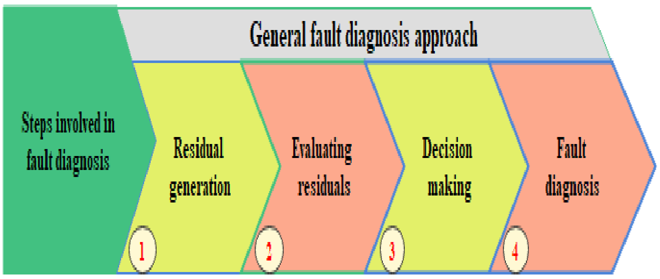



**Fig. 11.** Steps involved in general fault diagnosis approach

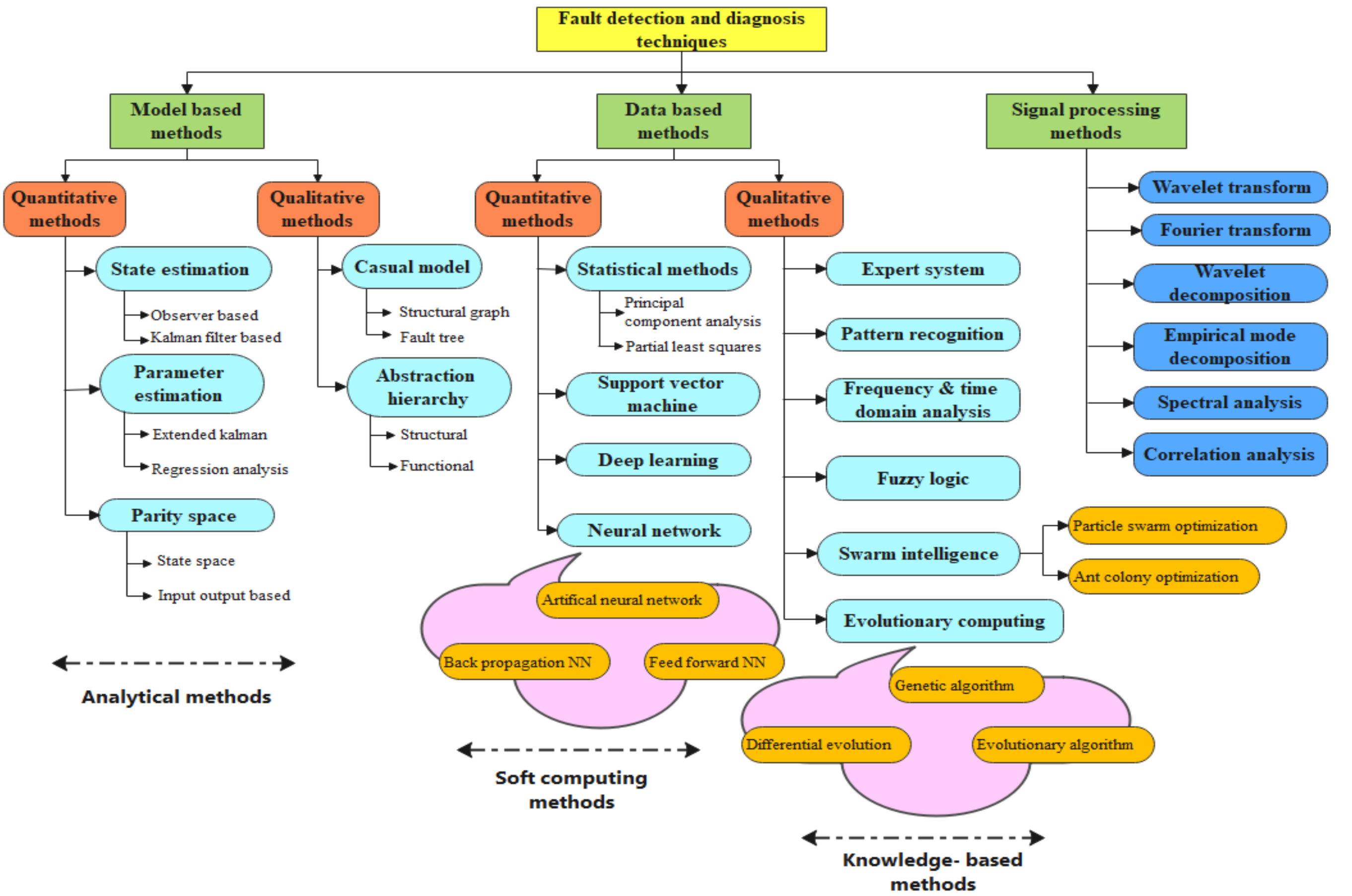



**Fig. 12.** Flowchart of various fault detection techniques

To reduce the computational burden with increased speed the online implementation of FS-MPC using FPGA was proposed in [78]. Finite set model-based predictive control (FS-MPC) algorithm proposed in [79] for single switch fault identification. Additionally, measurements and calculations synthesized for the control can be preserved for the fault detection process.

Furthermore, MPC has been used to detect OC faults within a single fundamental cycle by comparing pre-computed states to actual observed states. However, the model-based approaches have complex mathematical models which are tedious for a non-linear system resulting in large modeling errors, parameter variation, noise and disturbances.

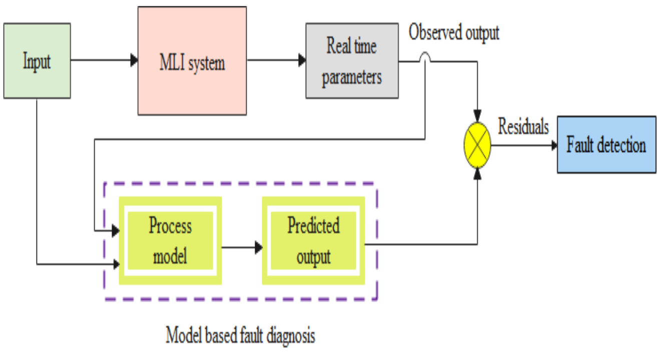



**Fig. 13.** Block diagram of model-based FD approach

*4.2 Data-Based Methods*

The data-driven method is not based on mathematical models; rather, it is based on the learning of specific conditions associated with particular data. Any newly presented condition can be found using prior training for fault detection. In other words, data-based approaches are to use a huge amount of historical data gathered from the system under examination through machine learning or multivariate statistical models. The block diagram of the data-based FD technique is depicted in Fig.14. These approaches include pattern recognition, spectral analysis, support vector machine, and competitive learning based on machine learning, artificial intelligence, neural network, fuzzy logic. The advantage of the data-driven method is faster fault detection, easy to implement, robust, and requires less prior knowledge and computational complexity.

However, the accuracy of the FD depends on the quality and quantity of the data [80]. To detect the fault, the fault features should be extracted from different signals obtained from the raw measurement of data in the time domain or frequency domain. A variety of techniques can be used to extract the fault features such as principal component analysis (PCA), support vector machine (SVM), and machine learning tools like random forest (RF), discriminant analysis (DA), decision tree (DT), k-nearest neighbor (KNN).

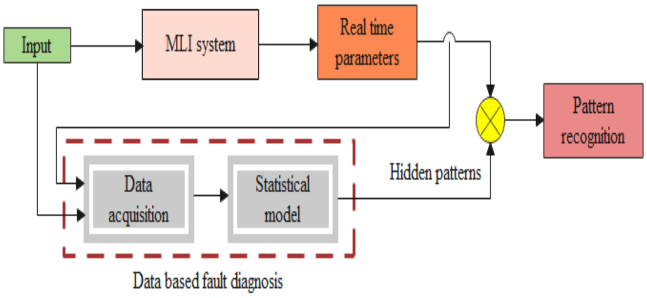



**Fig. 14.** Block diagram of data-based FD approach

*4.2.1 Principal Component Analysis (PCA) Technique*

PCA is a statistical technique that acquires the most significant components while reducing the less important ones. It is used to extract the fault features and to reduce the dimension of the principal components. Orthogonal transformation is used to extract the principal components from the source data. To improve the fault diagnosis accuracy of CHB MLI, a principal component analysis and multiclass relevance vector machine (PCA-mRVM) approach is suggested in [81]. This approach is complex and difficult to train the mRVM model for the higher number of levels. Moreover, the requirement of an additional sensor increases the cost of the system.

Partial least squares regression is another statistical technique; it determines the regression analysis by projecting the expected and observed variables to a new space [82]. It necessitates a large number of components for prediction, which is ineffective. It is a less efficient method than PCA. It begins with a least-squares calculation and then does an orthogonal decomposition of the measurement space. A method for detecting OC fault and identifying faulty switches using the LS-PWM technique is presented in [83]. The proposed detection method accurately identifies the faulty switches within the H- bridge employing switching logic based on their switching state (on/off status), output voltage, and current characteristics.

*4.2.2 Support Vector Machine (SVM) Approach*

SVM is the most widely used machine learning technique for the classification of data. The different fault features are represented on a hyperplane in a three-dimensional space. To achieve sample classification, SVM uses a kernel function to transform input vectors nonlinearly into a high dimensional feature space and create the optimal separating hyperplane as shown in Fig.15. A new SVM control technique is proposed in [84] to more precisely identify one or more defective cells. It applies to any number of CHB MLI levels to detect OC fault. However, incorporating a voltage sensor to monitor the output voltage of each cell adds to the circuit cost. The PCA-SVM-WE-based open circuit fault detection for single and multiple switches was discussed in [85], which minimizes the fault detection time with enhanced accuracy of 99.9%. And, it was shown that the PCA-SVM combination gives better accuracy compared to other machine learning approaches. However, the fault detection time is quite high in the PCA-SVM approach.

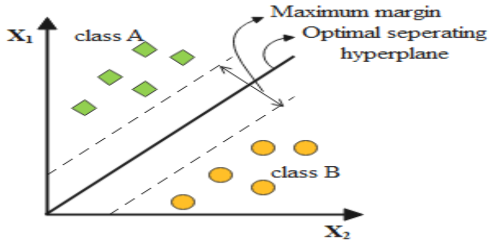



**Fig. 15.** Data classification in SVM

*4.3 Signal Processing Methods*

Faults in the MLI system are projected to have an enormous impact on the terminal output characteristics, particularly distortion in the current and voltage waveforms. Anomalies in the output signal are typically observed using signal processing methods. The block diagram of the signal processing method is shown in Fig.16.

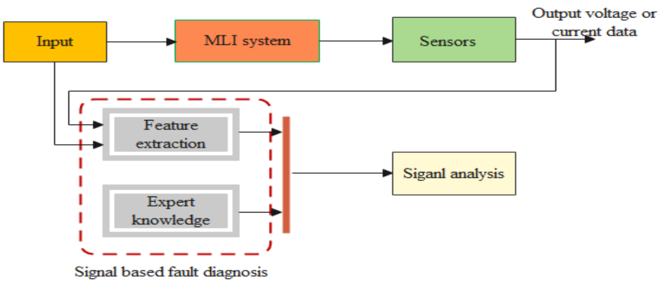



**Fig. 16.** Block diagram of signal processing method

The Fourier transform or wavelet transform is used to examine the signal, which can be used to identify faults. Signal processing methods are further classified into the time domain, frequency domain, time, and frequency domain analysis. Fast Fourier transform (FFT) and Discrete Fourier transform (DFT) are frequency domain techniques that are not suitable for non-stationary signals. Non-stationary, intermittent, and transient signals can be scrutinized mathematically using the wavelet theory, which uses small waves termed wavelets as its constituent parts.

Wavelet transform (WT), discrete wavelet transforms (DWT), and short-time Fourier transform (STFT) is time and frequency methods. Time-varying or discrete signals can be analyzed using the discrete wavelet transform (DWT) method [86]. It automatically removes both low and high-frequency components from the signal. The DWT technique is investigated for NPC and CHB MLI in [87] and [88]. The Wavelet packet decomposition (WPD) decomposes the signal into two components at each node, whereas DWT decomposes the signal into a single coefficient which is not optimal in transient conditions or at high frequencies. An analog circuit fault detection method based on the combination of neural networks and wavelet transforms as described in [89], in which the wavelet transforms were used to eliminate the noise from the sampled signals and PCA was used to reduce data dimension.

A new fault detection method based on the adaptive electrical period partition (AEPP), employing maximal overlap DWT (MODWT) and park's vector modulus (PVM), random forest (RF) method is presented in [90] for NPC inverter. AEPP is used to select the electrical period from real-time data and decompose it using MODWT and PVM technique which is preserved for fault diagnosis. Hence, the proposed RF technique yields the maximum fault diagnosis accuracy of 99.38%.

*4.4 Soft Computing Methods*

Recently, soft computing techniques like artificial intelligence (AI), machine learning (ML), neural network (NN), fuzzy logic (FL), adaptive neuro-fuzzy inference system (ANFIS) pose a revolutionary breakthrough in the field of fault diagnosis. All of these strategies rely on data to train the network. The soft computing algorithms are trained to understand the relationship between input and output parameters of the system. Hence the accuracy of the fault detection and classification is highly dependent on the data set used for training and testing [91]. The data set is derived from the output voltage and current, or both, during the system's normal and abnormal states. The dataset can be obtained by either an experimental setup or simulated results. In general, 70% of data sets are required for training, while 30% of data sets are required for testing. However, raw datasets cannot be used directly for fault diagnosis; consequently, they need to be processed through conditioning phases [92], [93].

Feature extraction, neural network classification, fault diagnosis, and reconfiguration are the four stages in the fault diagnosis approach [94]. Fault feature extraction is the primary step of screening and decreasing the original fault signal (raw data obtained from inverter output) which is the necessary condition for fault diagnosis. Further, the classification of a neural network is based on AI and FL. The AI classification algorithm includes artificial neural network (ANN), decision tree (DT), SVM, and kNN. Artificial intelligence methods are well suited for real-time implementation because of their accuracy and low computational burden whereas fuzzy logic is a rule-based method that is much expensive which limits its real-time implementation [95]. The neural network uses both normal and abnormal data as input and produces binary output as 0 and 1. Hence, fault diagnosis and switching patterns are predicted based on the binary output.

*4.4.1 Artificial Neural Network (ANN) Technique*

ANN is used for the classification of data to recognize the pattern. Fig.17 depicts an ANN architecture with a set of input layers, hidden layers, and output layers. The hidden layer and neuron in each layer should be selected based on the problem to be examined [96]. The steps involved in ANN techniques are shown in Fig.18. A new fault detection method based on a single ANN model for asymmetric CHB MLI was investigated in [97], where THD, mean value of output voltage were used as input parameters to train the ANN model. Another technique based on AI is presented in [98] to detect both OC & SC faults. It takes about 100ms to clear an OC fault, clearing time is quite high.

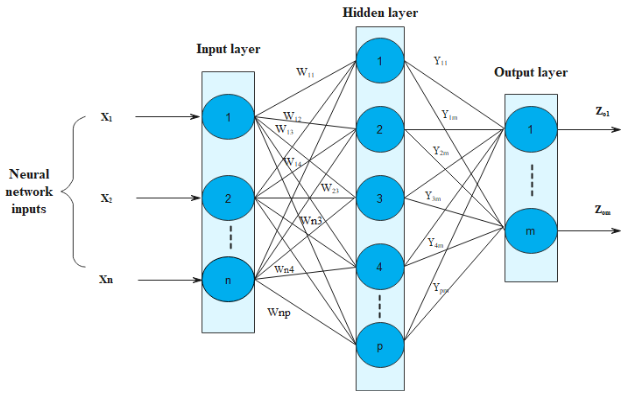



**Fig. 17.** Artificial neural network structure

Fault diagnosis of CHB MLI using discrete wavelet packet transform-based (DWPT) for feature extraction and ANN for fault classification has been presented in [99] under dynamic load conditions. DWPT gives better resolution than other techniques because it effectively decomposes coefficient to extract fault features. The open-circuit fault detection using machine learning techniques is proposed in [100] in which the DWT+DT approach gives the shortest fault detection time with the highest accuracy. ANN-based fault diagnosis of CHB MLI is implemented [101] using the DWT technique to identify and locate the specific faulty switch accurately within 10ms. Moreover, it reduces the size of input neurons of ANN. The FFT-RPCA-SVM approach is present in [102] for detecting open and short circuit faults in power switches in inverter-fed induction motors with an average classification accuracy of 99.9 percent. In [103] open-circuit fault diagnosis system for CHB MLI using the Wavelet decomposition method was proposed. Wavelet is used to extract fault features from inverter output voltage and current signals.

Fault classification accuracy of 99.9% has been achieved using ANN. The fault diagnosis using the neural network is trained with four different algorithms proposed [104] that radial basis neural network performs better than the ordinary neural network gives lowest mean square error. For better understanding, the neural network fault diagnostic strategy is shown in Fig.19.

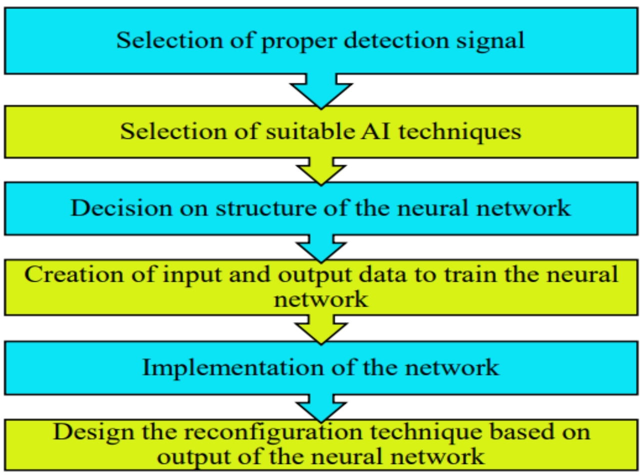



**Fig. 18.** Flowchart of ANN techniques

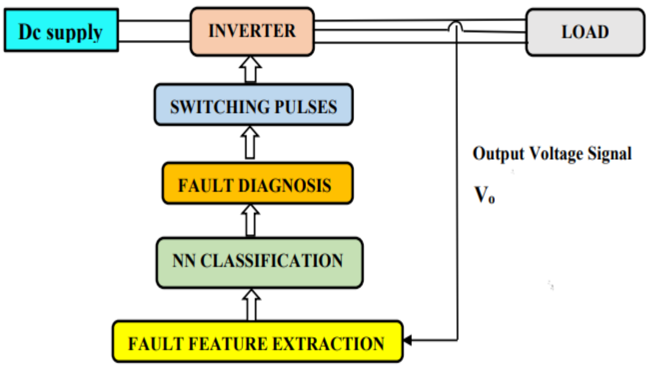



**Fig. 19.** Neural network fault diagnostic method

In [105] the backpropagation NN-based fault detection system is proposed for various switch faults like an open circuit, short circuit, and gate drive fault. Although, the feature extraction method is not discussed in this work. However, these approaches necessitate a substantial dataset for algorithm training and have high computing requirements. An optimization strategy is used during ANN training to minimize the weight value of the node to increase the ANN's training speed. Optimization algorithms such as particle swarm optimization (PSO), genetic algorithm (GA), modified genetic algorithm (MGA), and cuckoo search algorithm (CSA) is used to optimize NN and to reduce mean square error [106]. To effectively optimize ANN training, the metaheuristic method such as PSO and GA are extensively used. To achieve faster training, the weight and bias values of the neural network are tuned using the MGA technique is presented in [107]. THD varies for varying fault condition and utilized as an input parameter to train the network.

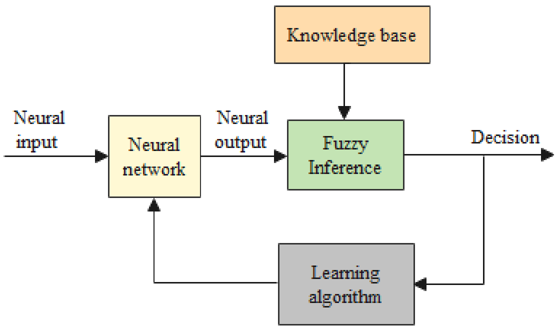



**Fig. 20.** Block diagram of Neuro-fuzzy system

*4.4.2 Fuzzy Logic (FL) Based methods*

This technique is based on a set of rules that converts the appropriate input variable into linguistic (output) variable (fuzzification). The significant aspect of FL, which is employed in a variety of applications, is its ability to recognize nonlinear relationships between selected input and specified output. Fuzzification, interpretation, and defuzzification are the three basic steps of fuzzy logic [108]. In [109], the fuzzy logic method is utilized to identify single and multiple switch open circuit failures, reducing computational complexity and implementation effort when compared to other soft computing techniques. In contrast, [110] proposes a fault diagnostic technique that uses phase current as an input parameter to detect and locate intermittent single and multiple switch faults. However, due to the imperfect input, the rate of identification and detection is low. The author in [111] proposes a fuzzy logic-based fault detection approach for detecting and classifying various switch faults in an inverter that considers parameter variation and non-linearities in the input. Hence, FL provides an effective method of fault detection that does not require large amounts of training data or extra observations. The performance comparison of various neural network algorithms is illustrated in Table 5 and corresponding charts as shown in Fig.21.

*4.4.3 Hybrid and ANFIS Technique*

When two fault detection techniques are combined into a single algorithm, it is known as a hybrid technique. Usually, hybrid techniques are used for precise fault detection, to recognize multiple faults, and to reduce computational complexity. A hybrid intelligent algorithm using a back propagation (BP) neural network was proposed [112] to identify the location of the fault. Wavelet packet transforms with PCA is used to extract fault features from raw data. The training of this algorithm is very simple and has 90% accuracy. In [113], a combination technique of wavelet analysis and SVM is used to extract fault features and classify open circuit faults. The accuracy of 98.1% has been obtained using the hybridized technique. Recently, the hybridized multiclass neuro-fuzzy classifier (MC-NFC) based fault detection and classification technique was introduced in [114] for the photovoltaic array to distinguish five kinds of fault. Also, the MC-NFC output is compared with the ANN classifier, which shows the superiority of the MC-NFC.

An adaptive neuro-fuzzy inference system (ANFIS) is one in which the fuzzy inference system is integrated into the architecture of an adaptive neural network. ANFIS control is used to improve the performance of FL and reduce computational complexity. The block diagram of the neuro-fuzzy system is illustrated in Fig.20. The ANFIS control doesn't suffer from uncertainties, noise, and disturbances. In [115], an effort is made to locate a faulty switch in a multilevel inverter using the ANFIS approach. FFT techniques are used to extract fault features from output voltage and THD values, which are then used to train the ANFIS network. It requires fewer training data, reducing network complexity, and achieving a satisfying mean square error. In [116], the NN optimization employs joint approximative diagonalization of eigen matrix (JADE) and independent component analysis (ICA) algorithm to reduce the size of an input to the NN. The proposed algorithm minimizes the training time of the neural network. In [117], the attempt is made to enhance the diagnostic accuracy of deep feedforward network (DFN) through compression of redundant data using WT.

*4.5 Overview of Fault Detection Techniques*

This section examines each approach on a unified platform to assess the performance of various fault detection strategies. The following characteristics have been examined and are extensively addressed: 1) Accuracy: This is the key aspect of any detection approach and is evaluated based on the precision of the fault detection criteria, the selection of detection variables, and the performance under all situations, 2) Approach: Indicates the overall technique that used to find faults, 3) Ability to locate the fault: The ability of the method to identify the exact fault location, allowing maintenance simple and effective, 4) Implementation complexity: Indicates the simplicity with which the proposed approach can be implemented into the existing system, 5) Diagnosis capability: Indicates whether the technique is capable of distinguishing between multiple faults with the same pattern efficiently, 6) Fault detection time: Time required to accurately identify a fault.

**Table 5.** Performance comparison of neural network-based algorithm

| Reference | Algorithm | Diagnosis accuracy (%) | Sampling time |
|---|---|---|---|
| [102] | FFT-RPCA-SVM | 99.9 | 8.7ms |
| [116] | JADE-ICA-NN | 95.1 | 4s |
| [117] | DFN-WT | 97 | 2ms |
| [118] | FFT-NN | 91 | 35s |
| [119] | Wavelet-NN | 93 | 19s |
| [120] | FFT-ANN | 99.9 | 10ms |
| [121] | PSO-NN | 99.8 | 20ms |
| [122] | LMA-ANN | 97 | 39s |

In this regard, the advanced detection strategies investigated in this study outperform standard protective devices in terms of detection accuracy, and these techniques may be employed as alternative detection schemes in MLI systems. Among the numerous fault detection techniques, ANN, ANFIS, and SVM have been recognized as potential options for scrupulous fault detection.

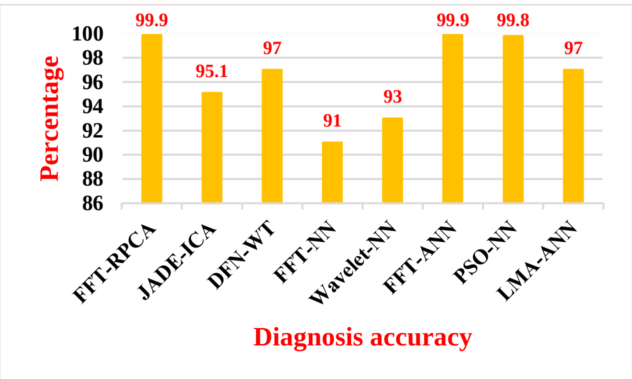



**Fig. 21.** Comparison of neural network algorithm with diagnosis accuracy

## 5. Fault Tolerant Control Methods İn Multilevel Inverter

The capacity of a system to continue to work in the context of faults or malfunctions is referred to as fault tolerance. The multilevel inverter incorporates a large number of switches and sources for its energy conversion. Further, the number of switches increased with increasing levels, which increases the frequency of a fault. As a corollary, the reliability of MLI falls significantly. To enhance the power quality and inverter reliability, it is extremely important to diagnose faulty switches and establish a fault tolerant control (FTC) approach [16]. The FTC strategy should address the following MLI system challenges such as, mitigating various fault types, maintaining post fault output power, being cost-effective, non-utilization of inherent redundant paths at middle voltage level to achieve maximum efficiency, minimizing component count, preventing the usage of bidirectional switches, difficulty to transmit load current in the event of an overload, equal use of voltage sources. Hence, this section focuses on the fault-tolerant control of various MLI to overcome these challenges and to analyze the control based on the location and kind of switch failure. Methods of fault-tolerant control for multi-level inverters are classified as shown in Fig.22 and the fault tolerant strategies for different levels of fault are depicted in Fig.23.

### *5.1 Fault Tolerant Control Methods in NPC MLI*

The 5 level NPC MLI architecture proposed in [123] can withstand both open circuit and short circuit fault on its switches. The architecture provides partial and complete solutions to faults with self-voltage balancing capability under fault conditions. However, the architecture failed to provide an overload current sharing capability, the utilization of bidirectional switches increases the switching losses.

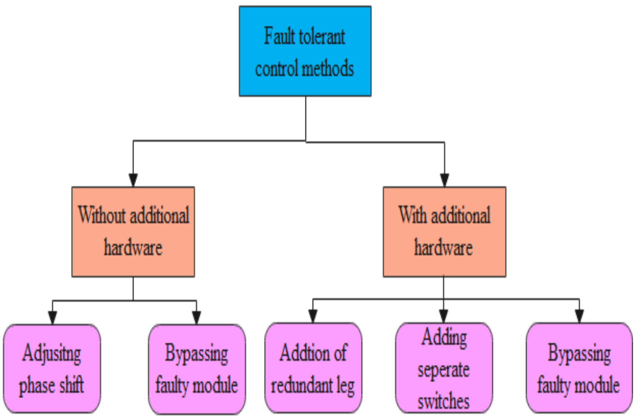



**Fig. 22.** Fault tolerant control methods

On other hand, the NPC MLI structure presented in [124] is the advancement of the structure depicted in [123] which reduces the utilization of bidirectional switches with novel redundant leg architecture. It also provides the overload (OL) current sharing capability with increased inverter efficiency. Moreover, the complexity of the structure increases with redundant leg architecture.

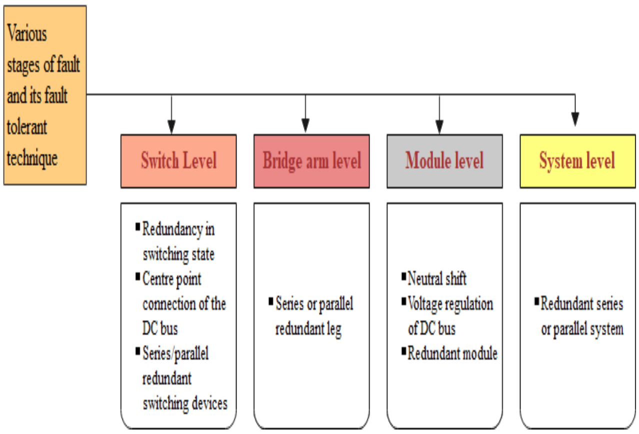



**Fig. 23.** Various levels of the fault and its tolerant methods

Other challenges with NPC MLI include neutral point voltage balancing and uneven power loss distribution; these shortcomings result in lower output voltage, which is unsatisfactory for applications that demand maximum output power. For PV applications, in [125] the new FTC structure was suggested to withstand single switch faults and energy balancing capacity under partial shading conditions. This structure includes three-level NPC with two h-bridge inverters and a bidirectional switch to tolerate source and switch OC/SC faults. However, the suggested approach can tolerate only selected switch faults, resulting in only partial fault tolerance with lower output power. In [126] the fault-tolerant control using an additional leg was considered. Furthermore, the addition of leg was employed to accomplish neutral point voltage balance in normal conditions. However, in addition to an extra leg, bidirectional switches were required for each phase which raised the system cost and conduction losses.

The common drawback in the previously stated FTC techniques is their inability to cover multiple switch failures in different locations. To overcome the shortcomings stated above, a multiple switch fault-tolerant scheme is proposed in [127] that employs a redundant leg with only six IGBT switches. The proposed topology utilizes only two switches to tolerate open circuit and short circuit fault which is the more advantageous in FTC. Besides, it doesn't include bidirectional switches which in turn reduces the power losses and increases the efficiency of the inverter.

Another key challenge in MLI is equal voltage source utilization. The symmetric architecture presented in [128] successfully tolerates single and multiple switch faults with optimal voltage source utilization under faulty conditions. It utilizes bidirectional switches to withstand a single switch fault in all switches of the main inverter. However, there is a greater reduction in output voltage which diminishes the inverter efficiency. A fault-tolerant MLI is suggested in [129] to improve the efficiency of the MLI even while preserving output power. The topology employs redundant leg to sustain OC and SC faults in single and multiple switches for various fault locations. However, utilizing a larger number of switches increases the system's cost and complexity. Another approach is that manipulating inherent redundant switching states to tolerant multiple switch faults.

Recently, SVM has been employed in fault-tolerant techniques owing to its advantages of producing the same voltage vector using redundant switching states. The redundancy in the switching state is utilized to achieve fault tolerance at a low modulation index [130]. Inactive neutral point clamped (ANPC) inverter, the clamping diodes were replaced with active switches. It has a greater number of zero switching states which aids in balancing the loss distribution by employing a variety of current pathways. The author in [131], [132] suggested an OC fault diagnostic and tolerance control approach for grid integrated hybrid ANPC inverters using optimal carrier-based pulse width modulation. This approach is simple and can handle up to four switch faults in single phase without the need for extra hardware. However, in all the above discussed methods are failed to provide both multiple OC and SC fault. In [133], an effective fault tolerant control approach for ANPC MLI is developed to tolerate multiple OC & SC faults without the insertion of any extra hardware. The fault tolerant control is performed by modifying the vector mapping, introducing a unique switching sequence, and adjusting the reference voltage. To achieve fault tolerance, SVM-based fault tolerant algorithms need complicated switching sequences that are restricted in a number of levels.

### *5.2 Fault Tolerant Control Methods in FC MLI*

FCMLI architecture offers greater switching state redundancy per voltage level than DCMLI besides providing additional possibilities for fault tolerance and capacitor voltage balancing. In [134], the fault tolerant control for FC MLI is presented to tolerate single switch SC fault without adding additional hardware components. The SC fault is recognized by the hardware protection circuit, and the fault-tolerant operation is carried out by the algorithmic-based controller. However, the architecture is not capable of tolerating multiple switch faults and a significant reduction in output voltage under faulty conditions. In [135], the fault tolerance is performed by shorting the faulty switch and modifying the control strategy. This architecture employs a greater number of switches and a pair of bidirectional switches in each leg, which raises the cost. However, fault tolerance at higher voltage levels is difficult to establish. In [136], switching strategies are utilized to tolerate a single switch fault. However, after reconfiguration, the proposed FC inverter is not able to produce a pre-fault voltage level.

A fault-tolerant design of FC MLI is proposed in [137], which utilizes a bypass switch to each phase to withstand an open circuit failure, although it raises the system's cost. To withstand the OC fault, the fault tolerant control was devised [138] by configuring the circuit to a two-level inverter without adding new components. However, the proposed scheme can tolerate only the upper switch fault, and also the magnitude of the output voltage decreases resulting in lower efficiency. This is unacceptable in applications requiring continuous power. Thus, fault identification and switching sequence reconfiguration are essential to sustaining the same output voltage as in a healthy condition.

*5.3 Fault Tolerant Control methods in CHB MLI*

A cascaded h-bridge multilevel inverter comprises isolated dc sources and power semiconductor switches. Each module has four thyristors (T1-T4) and diagonal thyristors are responsible for a level generation. Due to the h-bridge's series connection, the dc sources must be isolated to provide the full output voltage. The CHBMLI facilitates the use of DC sources with different magnitudes and generates a wider range of output voltage levels. The primary approach is to bypass the faulty switches and then employ other healthy inverter switches in the CHBMLI to compensate for the faulty unit. Usually, the relay is connected to each module to isolate and bypass the faulty cell. The solution provides the system to operate continuously but with reduced voltage [139]. In [140], relays were added to a traditional CHB inverter to make it fault-tolerant (FT). Even though, in the reconfiguration process, it was observed that the healthier switches had larger blocking voltages, resulting in increased switching stress. The drawbacks of [140] were resolved in [141]. This topology, however, necessitates the use of an additional non-fault-tolerant CHB for polarity generation. Furthermore, the topologies presented in [140] and [141] fail to provide the same power when multiple switch failures occur. Another solution is to provide an auxiliary module to overcome the limitations of the relay to generate a balanced output voltage. In [142], an ANN-based fault-tolerant system for PV-fed CHBMLI is presented which distributes power to the load even under failure and partially shaded situations.

The proposed algorithm can tolerate different types of faults (OC & SC) in both MLI and PV systems (partial shading). This proposed method employs an auxiliary module, the operation of which is regulated by two switches. However, the topology proposed in both [142] and [143] adds weight, expense, and inverter losses. The novel generalized architecture provided in [144] comes with a new level shifted carrier PWM approach that successfully uses the irregular (faulty) voltage level to power emergency loads. The suggested topology is capable of operating in both symmetric and asymmetric modes, as well as being fault resilient. It employs a fewer number of conducting switches for all voltage levels, reducing power loss and increasing inverter performance. Furthermore, the suggested topology allows for the generation of skipped voltage levels at the output.

In [145], a new fault-tolerant structure is proposed by adding five unidirectional switches to a half-bridge inverter, which can tolerate a single switch fault with reduced output power. In [146], fault-tolerant control of CHB MLI based on neutral shift was developed utilizing the LS PWM approach. In this study, the fault is classified as type 1 (both OC and SC) and type 2 (OC alone). Tolerating a type 1 fault requires the use of a neutral shift mechanism, whereas a type 2 fault requires the employment of a rotational switching scheme. However, as the degree of complexity increases, the reconfiguration of the switching system becomes more difficult for higher levels. The faulty switch is effortlessly bypassed in [147] by altering the carrier frequency and modulation ratio. This approach is only suitable for cascaded MLI with carrier phase shifting PWM. In [148] faulty switches are classified into three groups depending on fault level and location. These groups are referred to as clusters. Cluster I faults include double switch faults in different h-bridges and groups, and the FTC algorithm is built for each cluster and validated for cluster I type faults. The suggested approach successfully uses the healthy switch in the faulty location and minimizes the voltage level reduction during the fault. However, the computing complexity is increased by the independent control algorithms for each group. To compensate for loss voltage levels under single switch failure conditions, a cross-coupled (X)- CHB module is used in association with a normal CHB module [149]. However, to compensate for the missing voltage level in a single module, an additional eight switches in the X-CHB are required, making the circuit more complicated.

*5.4 Fault Tolerant Control Methods in Hybrid MLI*

The hybrid fault-tolerant control is used to increase inverter performance by integrating redundant inverters. In [150], a resilient five-level hybrid (combination of FC+NPC+CHB) FT structure is presented. It can handle open-circuit and short-circuit failures in single and multiple switches while preserving output power and post fault voltage levels. However, it requires a greater number of switches for a higher level, which increases the cost and complexity of the system. In [151], a hybrid five-level fault tolerant architecture with an equal number of switches in the main inverter and the redundant leg is presented. It can tolerate single and multiple switch faults with preserved output power and self-balancing of the capacitor.

The hybrid construction employs FC and CHB in the primary inverter, while ANPC in the redundant leg maintains output power in all faulty scenarios. The equivalent number of redundant leg switches, which in turn raises the overall device count. Furthermore, it can only handle open circuit failures. In [152], proposes a unique transistor clamped cascaded h-bridge architecture for tolerating the OC and SC fault on single switches while improving reliability. To increase performance, one leg of the CHB inverter is replaced with an NPC leg, which offers voltage redundancy in the case of failure. Furthermore, the structure can withstand a capacitor failure, but with higher voltage ripples. The downsides of this topology are the utilization of four-quadrant switches and limited fault tolerance. The hybrid topology is described in [153] by combining an FC leg with a two-level CHB leg. The single switch fault in the FC and CHB legs is tolerated by adding an additional resonant leg and bidirectional switches, which increases conduction losses and adds complexity. Despite the inclusion of additional switches, the system is unable to endure multiple switch failures.

*5.5 Overview of Fault-tolerant Techniques*

This section provides an overview of several fault-tolerant control systems, difficulties, and solutions. Table 7 illustrates a comparison of several FTC approaches with their topology and switching strategies. Typically, faults in the MLI system are tolerated at the addition of extra switches or redundant legs. With the inclusion of hardware components, single and multiple switch faults can be tolerated.

**Table 6.** Comparison of various fault detection techniques

| Reference | Input data | Fault detection methods | Fault detection time | Complexity | Fault Identification | | Validation | |
|---|---|---|---|---|---|---|---|---|
| | | | | | OC fault | SC fault | Simu lation | Experi mental |
| [70] | Voltage and current signals | Voltage and current sensors | Less than one fundamental period | Simple | √ | * | √ | √ |
| [72] | Output voltage, current data with PWM signal | PS-PWM | About 5 fundamental period | Simple | √ | * | √ | √ |
| [73] | Voltage across each bridge | HCMV | Within one fundamental cycle | Simple | √ | * | √ | √ |
| [74] | Output voltage signal | Voltage measurement-PS PWM | 100$\mu s$ | Simple | √ | * | √ | √ |
| [75] | Output voltage data | Voltage& current measurement-LSPWM | <20$ms$ | Simple | √ | * | √ | √ |
| [76] | Pole voltage of each phase | Model-based-voltage measurement | Few milliseconds | Simple | * | √ | √ | * |
| [79] | Current signal | Finite set-MBPC algorithm | 49ms | Complex | √ | * | √ | √ |
| [81] | Output voltage of inverter & each bridge | PCA-mRVM | Within one fundamental cycle | Complex | √ | * | √ | √ |
| [98] | Output voltage & current | FFT-ANN | 10ms | Simple | √ | √ | √ | √ |
| [84] | Output voltage cell | Modified SVM | 1ms | Simple | √ | * | √ | √ |
| [90] | Current signal | PVM, MODWT, RF | # | Complex | √ | * | √ | √ |
| [98] | Output phase voltage | AI-GA | 100ms | Complex | √ | √ | √ | √ |
| [101] | Output voltage | DWT | 10ms | Simple | √ | √ | √ | √ |
| [103] | Output voltage and current | Wavelet decomposition -ANN | # | Complex | √ | * | √ | * |
| [112] | Output voltage | BP- NN | # | Simple | √ | * | √ | * |
| [14] | Output current | LS-PWM | # | Simple | √ | √ | √ | √ |
| [15] | THD & output phase current | THD waveform & normalization factor | # | Simple | √ | * | √ | * |

**Table 7.** Comparison of various fault-tolerant control methods based on switch fault

| Faults considered | Refer -ence | Description of the method | | | | Comments |
|---|---|---|---|---|---|---|
| | | Topology discussed | Switching technique | Parameters analysed | FTC methods | |
| Single switch fault | [125] | NPC | PD-PWM | Energy sharing analysis | Inclusion of bidirectional switches | The addition of series transformer makes system complexity |
| | [154] | Modified MLI | LSF | THD analysis, switching loss calculation | Using Bidirectional switches | Not easily extendable |
| | [155] | CMLI | Multicarrier sinusoidal PWM | Reliability analysis | Redundant switching methods | Failed to preserve post fault output voltage level |
| | [156] | Generalized MLI | Level shifted-SPWM | Reliability analysis using Markov's model | Redundant switching methods | Unidirectional and bidirectional switches are required to make complex circuitry. |
| Both OC & SC fault | [157] | CHB MLI | Variable frequency inverted sine carrier PWM | THD analysis | Based on CHB MLI structure | Output voltage magnitude was lowered due to an inner switch fault |
| | [134] | FC | PS-PWM | Capacitor voltage balancing | Algorithmic based controller | Hardware-based solution. Not suitable for higher levels |
| | [158] | CHB | Multicarrier PWM | THD and switching loss analysis | Rotating phase shift | Performance comparison between PS PWM & LS PWM techniques |
| | [123] | NPC | Multicarrier PWM | Capacitor voltage balancing | Using bidirectional switches | A partial solution to the fault |
| | [153] | FC | LS PWM | Post fault capacitor voltage balancing | Resonant leg and bidirectional switches | The use of bidirectional switches results in increased losses |
| | [146] | CHB | LS PWM | Power distribution among CHB module. | Neutral shift and rotational switching mechanism | Eliminate the use of redundant inverter for single switch fault. |
| | [143] | CHB | Space vector modulation | THD analysis | Auxiliary module | Finding the nearest vector is hard when there are several switch faults |
| | [159] | FC | LS PWM | Reliability analysis | Redundant leg | Causes unbalanced output voltage |
| Multiple switch fault | [127] | NPC | Carrier PWM | Power loss | Redundant leg with minimal switches | Suitable for multi-switch OC/SC fault. |
| | [132] | ANPC | IPDPWM with CBPWM | DC link voltage balancing | Using carrier-based PWM | The capability of handling up to four open switch faults without the use of redundant switches |
| | [150] | Hybrid-Conventional FC, NPC, CHB | LSPWM | Power loss | Hybrid resonant leg | Not extendable |

| | | | | | | |
|---|---|---|---|---|---|---|
| | [124] | NPC | LSPWM | OL current sharing analysis | Redundant leg | Not ideal for a higher number of levels |
| Module failure | [140] | Conventional CHB | Sinusoidal PWM | Reliability evaluation, Power loss. | Using relay | Four relays were used which increases the cost of the system. |
| | [142] | CHB | POD PWM | - | Auxiliary module | Not ideal for higher levels. Requires more data set for training. |

It is mostly used for critical applications. The use of redundant switching states is also an effective way to tolerate the fault; moreover, redundancy comes with the inclusion of power switches. These solutions, however, raise the total cost and complexity of the system.

Another option based on software redundancy is the carrier-based PWM approach, which is commonly used to withstand numerous switch faults without the need for additional hardware. Following the occurrence of a fault, the switching signal is reconfigured. Because of its simplicity and cheaper cost, this strategy is more attractive. Hybrid approaches are typically used for complicated systems that require fault-tolerant control with higher voltage levels. However, the reliable fault tolerant control strategy should tolerate the multiple switch fault, with reduced components and preserved post fault output power.

## 6. Applications of the Fault Tolerant Multilevel Inverter

Reliability is one of the major concerns as the multilevel inverter used in critical applications like high power industrial drives, grid-connected applications, battery energy storage systems, and photovoltaic applications [160]. The inverter's reliability is mostly determined by its performance. If anyone of the inverter switch fails, the inverter fails to operate causes huge production losses. Hence, the fault diagnosis and fault tolerant control methods of MLI are invasive in applications. The multilevel inverter has a distinct advantage, particularly when working with PV applications. The CHB MLI has provided a significant solution to the issue of renewable-based energy production. This structure provides an effective response to power quality, multiple independent dc sources, and the ability to achieve maximum power point tracking (MPPT). PV strings can be linked to each dc-link capacitor independently, and the multilevel output voltage waveforms can be readily enhanced. CHB MLI have been described as an interesting solution in a PV system for these factors. Also, the following references examine the development for ANN-FD to be used in PV-based multilevel inverters [161].

In [162] the importance of fault detection in PV systems and the various recent fault detection methods have been discussed and it also emphasized fault detection method with locating fault points. In [125], the hybrid structure is proposed to tolerate the hotspot on one side of the PV string using the redundant switching strategy. The ANN technique was proposed in [163] to identify the partially shaded condition of the PV module. To predict the output parameters with high accuracy, the ANN should be trained regularly. In [164], [165], a fault tolerant inverter for PV application is proposed to tolerate multiple switches open circuit fault. Further, in all the above-mentioned topologies, even if the source and switches fail, the suggested inverter can continue to run at a lower level. An MLI with fault tolerant control for a three-phase induction motor for water pumping applications was presented in [166] to tolerate source fault and open circuit fault by modifying the switching strategy. The neutral shift-based control algorithm was proposed in [167] to optimize the consumption of energy stored in the battery and to improve fault-tolerant control of the CHB inverter. Hence, to enhance the reliability of the MLI, fault tolerant control should be emphasized.

## 7. Summary and Research Gap

The researchers were inspired to include fault detection and fault tolerant proficiencies in the MLI with lower switch counts due to augmented reliability concerns. It is of paramount importance to synthesize the multilevel inverter more reliable with fault tolerance. An in-depth examination of numerous fault occurrences and their catastrophic consequences using advanced fault detection and fault-tolerant control was drafted in this work. Furthermore, the fault detection approach was widely grouped into three major categories, and the techniques presented in each category were thoroughly evaluated using comparative analysis.

- The usual protective devices of the multilevel inverter are not dependable in detecting faults. Hence, advanced fault detection techniques come into existence to detect a fault in the MLI system more accurately.
- Data selection and fault feature extraction plays an important role in fault diagnosis. Hence, care must be given to select data that are not affected by multiple faults since the fault with the same signatures is difficult to distinguish with the same detection variables.
- The credibility of the fault diagnosis approach relies on the precision of fault detection and identification. In this regard, the knowledge-based fault detection methods are very much effective in detecting multiple faults without utilizing complex mathematical models.
- Indeed, the ANN approach has garnered the attention of researchers over the last decade primarily to its outstanding approximation of nonlinear functions, quick decision-making, and output independence.
- Among the various fault detection approaches, ANN and ML techniques provide classification accuracy greater than 90% in a short time. Despite that the ANN gives higher accuracy, the architecture utilizing a larger amount of datasets

for training has high computing requirements. Hence, optimization techniques are utilized to minimize the weight value of the neuron to enhance the training speed of the ANN.

- Optimization-based fault detection techniques are broadly utilized in the modern era due to their outstanding performance on non-linear systems. However, these types of fault detection algorithms have the potential to become future solutions for error-free fault detection.
- Despite detecting the fault, finding the exact location is also very hard. Hence, the fault detection system must be capable to locate the fault point for availing proper maintenance and mitigation.
- In this aspect, the improved power quality with harmonic elimination also increases the MLI's reliability. In considerations of optimal switching angle generation and harmonic elimination, the different PWM approaches were thoroughly examined. The challenges and solutions of modulation methods have been reviewed in this paper.
- In application domains, fault-tolerant control techniques are also needed to enhance power quality and reliability. Hence, fault-tolerant control of conventional and hybrid multilevel inverters based on hardware and software redundancy techniques has been deeply analyzed.
- Furthermore, the effective ways of tolerating single and multiple switch failures were examined. Also, the limitation of hardware redundancy and its possible solutions have been highlighted.
- Finally, the importance of fault-tolerant control in high power applications like photovoltaic systems, storage systems, grid-connected systems, and industrial drives was discussed.
- Overall, there is still a possible research gap in optimization-based fault detection and reliable fault mitigation techniques for MLI systems, and the arena will see significant developments in the upcoming years.

## 8. Conclusion

In modernized high power and medium voltage applications, multilevel inverters are inevitable. In this article, an extensive state-of-the-art assessment of fault detection and fault tolerant control techniques of multilevel inverters is presented. The various types of power switch fault and their impact on multilevel topology are discussed and the necessity of advanced fault detection methods are enlisted.

A comparison of different pulse width modulation techniques based on switching scheme, implementation complexity, and minimization of harmonics are also analyzed to improve the power quality and reliability of the multilevel inverter. Further, this work investigates the latest fault detection and isolation methods related to improving diagnostic accuracy. Among all the fault detection methods, the soft computing-based fault detection methods are highly accurate in terms of fault detection and classification. Further, these techniques also require research modification such as optimization of soft computing techniques for reducing computational complexity. Also, the various methods of fault tolerant control of multilevel inverter topologies and their challenges in mitigating the different levels of faults are extensively analyzed. Hence, on extensive study, a reliable fault-tolerant inverter with appropriate fault detection techniques plays a vital role in industrial applications. As a future scope, the fault tolerant multilevel inverter for single and multiple switch faults with improved reliability can be investigated.

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## References

[1] C. S. Lai, Y. Jia, L. L. Lai, Z. Xu, M. D. McCulloch, and K. P. Wong, "A comprehensive review on large-scale photovoltaic system with applications of electrical energy storage," *Renew. Sustain. Energy Rev.*, vol. 78, no. May, pp. 439–451, 2017, doi: 10.1016/j.rser.2017.04.078.

[2] R. Dogga and M. K. Pathak, "Recent trends in solar PV inverter topologies," *Sol. Energy*, vol. 183, no. April 2018, pp. 57–73, 2019, doi: 10.1016/j.solener.2019.02.065.

[3] "India on track to achieve 175 GW of renewable energy by 2022;Govt," 2019. https://energy.economictimes.indiatimes.com/news/renewable/india-on-track-to-achieve-175-gw-of-renewable-energy-by-2022-govt/71615089 (accessed Oct. 08, 2021).

[4] P. Kala and S. Arora, "A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications," *Renew. Sustain. Energy Rev.*, vol. 76, no. December 2016, pp. 905–931, 2017, doi: 10.1016/j.rser.2017.02.008.

[5] M. Pamujula, A. Ohja, R. D. Kulkarni, and P. Swarnkar, "Cascaded 'H' bridge based multilevel inverter topologies: A review," *2020 Int. Conf. Emerg. Technol. INCET 2020*, pp. 1–7, 2020, doi: 10.1109/INCET49848.2020.9154031.

[6] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002, doi: 10.1109/TIE.2002.801052.

[7] G. Muni Reddy and T. Gowri Manohar, "Multi level inverter based STATCOM for grid connected wind energy conversion system," *Int. J. Renew. Energy Res.*, vol. 7, no. 1, pp. 80–87, 2017.

[8] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, 2008, doi: 10.1109/TPEL.2008.2005192.

[9] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Convers. Manag.*, vol. 50, no. 11, pp. 2761–2767, 2009, doi: 10.1016/j.enconman.2009.06.032.

[10] P. O. , Kumar jagadish, Balawinder dingh surjan, "A review on multilevel inverter with reduced switch count," *IEEE Access*, vol. 8, pp. 22281–22302, doi: 10.1109/ICA-ACCA.2020.7778467.

[11] U. M. Choi, F. Blaabjerg, and K. B. Lee, “Study and handling methods of power IGBT Module failures in power electronic converter systems,” *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, 2015, doi: 10.1109/TPEL.2014.2373390.

[12] K. B, Senbakaraj, Periyasamy, and Poongkabilan, “THD Reduction in Multi Level Inverters based on Multicarrier Pulse Width Modulation Technique,” *Int. J. Eng. Adv. Technol.*, vol. 9, no. 4, pp. 1970–1977, 2020, doi: 10.35940/ijeat.d8994.049420.

[13] V. Anand and V. Singh, “Performance analysis of novel fault-tolerant multilevel inverter with a pristine methodology for fast and exhaustive real-time failure of switches,” *Int. J. Circuit Theory Appl.*, no. February, pp. 1–24, 2021, doi: 10.1002/cta.3073.

[14] J. H. Lee and K. B. Lee, “A Fault Detection Method and a Tolerance Control in a Single-Phase Cascaded H-bridge Multilevel Inverter,” *IFAC-PapersOnLine*, vol. 50, no. 1, pp. 7819–7823, 2017, doi: 10.1016/j.ifacol.2017.08.1058.

[15] P. Mehta, M. Kumar, and S. Sahoo, “Fault Diagnosis in Five-level CHB Inverter using Normalization Factor and THD Analysis,” *India Int. Conf. Power Electron. IICPE*, vol. 2018-Decem, no. 1, pp. 1–5, 2018, doi: 10.1109/IICPE.2018.8709547.

[16] B. Mirafzal, “Survey of fault-tolerance techniques for three-phase voltage source inverters,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5192–5202, 2014, doi: 10.1109/TIE.2014.2301712.

[17] Y. Shaoyong, X. Dawei, B. Angus, M. Philip, R. Li, and T. Peter, “Condition Monitoring for Device Reliability in Power Electronic Converters: A Review,” *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, 2010.

[18] J. Nicolas-Apruzzese, S. Busquets-Monge, J. Bordonau, S. Alepuz, and A. Calle-Prado, “Analysis of the fault-tolerance capacity of the multilevel active-clamped converter,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4773–4783, 2013, doi: 10.1109/TIE.2012.2222856.

[19] R. Venkatesh, P. Sharma, H. Siguerdidjane, D. Kumar, and H. D. Mathur, “Frequency Excursion Mitigation in a Multi-source Islanded Energy System Using Meta-Heuristic Optimization Strategies,” *2020 8th Int. Conf. Smart Energy Grid Eng. SEGE 2020*, pp. 148–152, 2020, doi: 10.1109/SEGE49949.2020.9182006.

[20] F. Richardeau, P. Baudesson, and T. A. Meynard, “Failures-tolerance and remedial strategies of a PWM multicell inverter,” *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 905–912, 2002, doi: 10.1109/TPEL.2002.805588.

[21] N. Soni, V. B. Borghate, S. Kumar Maddugari, D. Ambhore, and S. Sabyasachi, “A Simple Fault Tolerant Multilevel Inverter Topology,” *India Int. Conf. Power Electron. IICPE*, vol. 2018-Decem, pp. 2–7, 2018, doi: 10.1109/IICPE.2018.8709448.

[22] L. M. Halabi, I. M. M. Alsofyani, and K. B. Lee, “Multi Open/Short Circuit Fault-Tolerance using Modified SVM Technique for Three-Level HANPC Converters,” *IEEE Trans. Power Electron.*, vol. 8993, no. c, 2021, doi: 10.1109/TPEL.2021.3086445.

[23] V. Naumanen, J. Korhonen, J. Luukko, and P. Silventoinen, “Multilevel inverter modulation method to reduce common-mode voltage and overvoltage at the motor terminals,” *2010 IEEE 26th Conv. Electr. Electron. Eng. Isr. IEEEI 2010*, pp. 296–300, 2010, doi: 10.1109/EEEI.2010.5662221.

[24] Q. Yang, J. Qin, and M. Saeedifard, “Analysis, Detection, and Location of Open-Switch Submodule Failures in a Modular Multilevel Converter,” *IEEE Trans. Power Deliv.*, vol. 31, no. 1, pp. 155–164, 2016, doi: 10.1109/TPWRD.2015.2477476.

[25] J. Lee, H. Jang, S. Shin, K. Jang, and J. Jung, “Over temperature protection in power module for hybrid and electric vehicle,” *2016 IEEE Transp. Electrif. Conf. Expo, Asia-Pacific, ITEC Asia-Pacific 2016*, pp. 432–435, 2016, doi: 10.1109/ITEC-AP.2016.7512992.

[26] A. Sinha, K. Chandra Jana, and M. Kumar Das, “An inclusive review on different multi-level inverter topologies, their modulation and control strategies for a grid connected photo-voltaic system,” *Sol. Energy*, vol. 170, no. May, pp. 633–657, 2018, doi: 10.1016/j.solener.2018.06.001.

[27] H. Taghizadeh and M. Tarafdar Hagh, “Harmonic elimination of cascade multilevel inverters with nonequal dc sources using particle swarm optimization,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3678–3684, 2010, doi: 10.1109/TIE.2010.2041736.

[28] B. Mahato, R. Raushan, and K. C. Jana, “Modulation and control of multilevel inverter for an open-end winding induction motor with constant voltage levels and harmonics,” *IET Power Electron.*, vol. 10, no. 1, pp. 71–79, 2017, doi: 10.1049/iet-pel.2016.0105.

[29] T. H. A. Khaled El-Naggar, “Selective harmonic elimination of new family of multilevel inverters using genetic algorithms,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 5, pp. 89–95, 2007, doi: 10.1016/j.eswa.2010.07.021.

[30] K. Sundareswaran, K. Jayant, and T. N. Shanavas, “Inverter harmonic elimination through a colony of continuously exploring ants,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2558–2565, 2007, doi: 10.1109/TIE.2007.899846.

[31] S. Barkat, E. M. Berkouk, and M. S. Boucherit, “Particle swarm optimization for harmonic elimination in multilevel inverters,” *Electr. Eng.*, vol. 91, no. 4–5, pp. 221–228, 2009, doi: 10.1007/s00202-009-0135-9.

[32] V. Singh, G. V. V. R. Babu, and V. P. Singh, “New multi-level inverter topology with reduced number of switches,” *Proc. Int. Conf. Electron. Commun. Aerosp. Technol. ICECA 2017*, vol. 2017-Janua, pp. 462–467, 2017, doi: 10.1109/ICECA.2017.8203727.

[33] B. A. M.I.Sarwar, A.Sarwar, Shoeb , M.Tariq,

M.Fahad, R.Beig, "A Hybrid Nearest Level Combined with PWM Control Strategy: Analysis and Implementation on Cascaded H-Bridge Multilevel Inverter and its Fault Tolerant Topology," *IEEE Access*, vol. 9, pp. 44266–44282, 2021, doi: 10.1109/ACCESS.2021.3058136.

[34] Y. Park, D. Kim, J. Kim, and B. Han, "A New Scheme for Nearest Level Control with Average Switching Frequency Reduction for Modular Multilevel Converters," vol. 16, no. 2, pp. 522–531, 2016.

[35] H. Zhang, Y. Meng, L. Ning, Y. Zou, X. Wang, and X. Wang, "Fast and simple space vector modulation method for multilevel converters," *IET Power Electron.*, vol. 13, no. 1, pp. 14–22, 2020, doi: 10.1049/iet-pel.2019.0264.

[36] N. R. Jalakanuru and M. Y. Kiber, "Switching Angle Calculation By EP , HEP , HH And FF Methods For Modified 11-Level Cascade H-Bridge Multilevel Inverter," vol. 6, no. 12, pp. 69–75, 2017.

[37] H. Taghizadeh and M. Tarafdar Hagh, "Harmonic elimination of cascade multilevel inverters with nonequal dc sources using particle swarm optimization," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3678–3684, 2010, doi: 10.1109/TIE.2010.2041736.

[38] H. A. B. Siddique, A. R. Lakshminarasimhan, C. I. Odeh, and R. W. De Doncker, "Comparison of modular multilevel and neutral-point-clamped converters for medium-voltage grid-connected applications," *2016 IEEE Int. Conf. Renew. Energy Res. Appl. ICRERA 2016*, vol. 5, pp. 297–304, 2017, doi: 10.1109/ICRERA.2016.7884555.

[39] Q. Kartheryn, Jamer.J, Christian, "Hybrid Renewable Energy System based on Intelligent Optimization Techniques," *Int. Conf. Renew. energy Res. Appl.*, vol. 5, no. 20–23, 2016.

[40] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electron.*, vol. 6, no. 1, pp. 96–107, 2013, doi: 10.1049/iet-pel.2012.0228.

[41] J. Sun, S. Beineke, and H. Grotstollen, "Optimal PWM based on real-time solution of harmonic elimination equations," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 612–621, 1996, doi: 10.1109/63.506127.

[42] K. Yang, Z. Yuan, R. Yuan, W. Yu, J. Yuan, and J. Wang, "A Groebner Bases Theory-Based Method for Selective Harmonic Elimination," vol. 30, no. 12, pp. 6581–6592, 2015.

[43] H. Benbouhenni and O. Maurice, "Application of Five-Level NPC inverter in DPC- ANN of Doubly Fed Induction Generator for Wind Power Generation Systems," *Int. J. SMART GRID*, vol. 3, no. 3, 2019.

[44] M. Jafari, Z. Malekjamshidi, and M. R. Islam, "Optimal Design of a Multiwinding High-Frequency Transformer Using Reluctance Network Modeling and Particle Swarm Optimization Techniques for the Application of PV-Linked Grid-Connected Modular Multilevel Inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 5083–5096, 2021, doi: 10.1109/JESTPE.2020.3031731.

[45] M. B. Anurag, G. S. Thrinath, S. B. Karanki, and R. Yallamili, "Design of ZVS based high gain DC-DC converter for PV applications," *2016 IEEE Int. Conf. Renew. Energy Res. Appl. ICRERA 2016*, pp. 584–589, 2017, doi: 10.1109/ICRERA.2016.7884402.

[46] H. Turker, "Review of electric motors for grid connected integrated battery chargers in electric vehicle applications," *Int. Conf. Renew. energy Res. Appl.*, vol. 5, pp. 5–9, 2016.

[47] A. Ȧ Venkatakrishna, R. Ȧ Somanatham, and Ḃ M. S. R., "Phase Shifted and Level Shifted PWM Based Cascaded Multilevel Inverter Fed Induction Motor Drive," vol. 4, no. 1, pp. 350–354, 2014.

[48] N. L. H. Bang, N. V. Nho, N. K. T. Tam, and N. M. Dung, "A phase shifted PWM technique for common-mode voltage reduction in five level H-bridge cascaded inverter," *Proc. 2014 Int. Conf. Util. Exhib. Green Energy Sustain. Dev. ICUE 2014*, no. March, pp. 19–21, 2014.

[49] Y. Li, Y. Wang, and B. Q. Li, "Generalized Theory of Phase-Shifted Carrier PWM for Cascaded H-Bridge Converters and Modular Multilevel Converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 2, pp. 589–605, 2016, doi: 10.1109/JESTPE.2015.2476699.

[50] Y. L. Familiant and A. Ruderman, "Discussion of A Variable Switching Frequency PWM Technique for Induction Motor Drive to Spread Acoustic Noise Spectrum with Reduced Current Ripple," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, p. 5355, 2016, doi: 10.1109/TIA.2016.2618298.

[51] A. R. Kumar and T. Deepa, "Multilevel Inverters: A Review of Recent Topologies and New Modulation Techniques," *Proc. IEEE Int. Conf. "Recent Trends Electr. Control Commun. RTECC 2018*, pp. 196–203, 2019, doi: 10.1109/RTECC.2018.8625667.

[52] J. S. Choi and F. S. Kang, "Seven-level PWM inverter employing series-connected capacitors paralleled to a single DC voltage source," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3448–3459, 2015, doi: 10.1109/TIE.2014.2370948.

[53] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A Generalized Carrier-Overlapped PWM Method for Neutral-Point-Clamped Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9095–9106, 2020, doi: 10.1109/TPEL.2020.2969548.

[54] A. Radan, A. H. Shahirinia, and M. Falahi, "Evaluation of carrier-based PWM methods for multi-level inverters," *IEEE Int. Symp. Ind. Electron.*, pp. 389–394, 2007, doi: 10.1109/ISIE.2007.4374629.

[55] V. Jayakumar, B. Chokkalingam, and J. L. Munda, "A comprehensive review on space vector modulation techniques for neutral point clamped multi-level inverters,"

*IEEE Access*, vol. 9, pp. 112104–112144, 2021, doi: 10.1109/ACCESS.2021.3100346.

[56] L. Chaturvedi, D. K. Yadav, and G. Pancholi, "Comparison of SPWM,THIPWM and PDPWM technique based voltage source inverters for application in renewable energy," *J. Green Eng.*, vol. 7, no. 1–2, pp. 83–98, 2017, doi: 10.13052/jge1904-4720.7125.

[57] S. M. Kim and K. B. Lee, "A Modified Third Harmonic Pulse-Width Modulation for Reduced Switching Loss in Cascaded H-Bridge Multilevel Inverters," *IFAC-PapersOnLine*, vol. 52, no. 4, pp. 472–476, 2019, doi: 10.1016/j.ifacol.2019.08.255.

[58] B. Tan, Z. Gu, K. Shen, and X. Ding, "Third harmonic injection SPWM method based on alternating carrier polarity to suppress the common mode voltage," *IEEE Access*, vol. 7, pp. 9805–9816, 2019, doi: 10.1109/ACCESS.2018.2890014.

[59] R. Maheshwari, S. Busquets-Monge, and J. Nicolas-Apruzzese, "A Novel Approach to Generate Effective Carrier-Based Pulsewidth Modulation Strategies for Diode-Clamped Multilevel DC-AC Converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7243–7252, 2016, doi: 10.1109/TIE.2016.2538198.

[60] S. Das and G. Narayanan, "Novel switching sequences for a space-vector-modulated three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1477–1487, 2012, doi: 10.1109/TIE.2011.2163373.

[61] R. S. Yallamilli and M. K. Mishra, "Power management of grid connected hybrid microgrid with dual voltage source inverter," *2016 IEEE Int. Conf. Renew. Energy Res. Appl. ICRERA 2016*, vol. 5, pp. 407–412, 2016, doi: 10.1109/ICRERA.2016.7884370.

[62] H. Benbouhenni, Z. Boudjema, and A. Belaidi, "DFIG-based WT system using FPWM inverter," *Int. J. Smart Grid-ijSmartGrid*, vol. 2, no. 3, pp. 142–154, 2018, [Online]. Available: https://www.ijsmartgrid.com/index.php/ijsmartgridnew/article/view/16.

[63] M. Tarafdar Hagh, H. Taghizadeh, and K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, 2009, doi: 10.1109/TPEL.2009.2022166.

[64] B. A. M.sarwar, A.sarwar, Shoeb, M.Tariq, M.Fahad, R.Beig, "A Hybrid Nearest Level Combined with PWM Control Strategy: Analysis and Implementation on Cascaded H-Bridge Multilevel Inverter and its Fault Tolerant Topology," *IEEE Access*, vol. 9, pp. 44266–44282, 2021, doi: 10.1109/ACCESS.2021.3058136.

[65] P. M. Kumar and Y. V. P. Kumar, "Comprehensive Analysis on Critical Factors for the Operation of Advanced High Gain DC-DC Converters Used in Renewable Energy Applications," vol. 11, no. 3, 2021.

[66] A. Pyrkin, R. Cisneros, D. U. Campos-Delgado, A. Bobtsov, and S. Somov, "A model-based fault-detection strategy in DC/AC conversion," *IFAC-PapersOnLine*, vol. 53, no. 2, pp. 676–681, 2020, doi: 10.1016/j.ifacol.2020.12.814.

[67] J. Poon, P. Jain, I. C. Konstantakopoulos, C. Spanos, S. K. Panda, and S. R. Sanders, "Model-based fault detection and identification for switching power converters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1419–1430, 2017, doi: 10.1109/TPEL.2016.2541342.

[68] M. Salehifar, R. S. Arashloo, M. Moreno-Eguilaz, V. Sala, and L. Romeral, "Observer-based open transistor fault diagnosis and fault-tolerant control of five-phase permanent magnet motor drive for application in electric vehicles," *IET Power Electron.*, vol. 8, no. 1, pp. 76–87, 2015, doi: 10.1049/iet-pel.2013.0949.

[69] E. M. Cimpoeşu, B. D. Ciubotaru, and D. Ştefănoiu, "Fault detection and identification using parameter estimation techniques," *UPB Sci. Bull. Ser. C Electr. Eng. Comput. Sci.*, vol. 76, no. 2, pp. 3–14, 2014.

[70] J. Lamb and B. Mirafzal, "Open-Circuit IGBT Fault Detection and Location Isolation for Cascaded Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4846–4856, 2017, doi: 10.1109/TIE.2017.2674629.

[71] H. W. Sim, J. S. Lee, and K. B. Lee, "A detection method for an open-switch fault in cascaded H-bridge multilevel inverters," *2014 IEEE Energy Convers. Congr. Expo. ECCE 2014*, pp. 2101–2106, 2014, doi: 10.1109/ECCE.2014.6953680.

[72] M. T. Fard, W. A. Khan, J. He, N. Weise, and M. Abarzadeh, "Fast Online Diagnosis of Open-circuit Switching Faults in Flying Capacitor Multilevel Inverters," *Chinese J. Electr. Eng.*, vol. 6, no. 4, 2020.

[73] A. Anand, B. Akhil Vinayak, N. Raj, G. Jagadanand, and S. George, "A generalized switch fault diagnosis for cascaded h-bridge multilevel inverters using mean voltage prediction," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1563–1574, 2020, doi: 10.1109/TIA.2019.2959540.

[74] M. Shahbazi, M. R. Zolghadri, M. Khodabandeh, and S. Ouni, "Fast detection of open-switch fault in cascaded H-bridge multilevel converter," *Sci. Iran.*, vol. 25, no. 3D, pp. 1561–1570, 2018, doi: 10.24200/sci.2017.4371.

[75] M. Hassanifar, "Fast Detection and Localization of Open-Circuit Switch Faults in Nested Neutral Point Clamped ( NNPC ) Inverter," *Ieee*, pp. 8–13, 2020.

[76] M. Alavi, D. Wang, and M. Luo, "Model-based diagnosis and fault tolerant control for multi-level inverters," *IECON 2015 - 41st Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 1548–1553, 2015, doi: 10.1109/IECON.2015.7392321.

[77] H. Mirshekali, R. Dashti, H. R. Shaker, and R. Samsami, "A New Model Predictive Control Based Method for Control of Grid Connected Inverter Using Predictive Functional Control," *2020 8th Int. Conf. Smart Energy Grid Eng. SEGE 2020*, pp. 22–26, 2020, doi: 10.1109/SEGE49949.2020.9181896.

[78] J. A. Thomas, "Prediction of Heat Demand for

Building Energy Managers: An IoT and Control Perspective," *8th Int. Conf. Smart Grid, icSmartGrid 2020*, pp. 29–36, 2020, doi: 10.1109/icSmartGrid49881.2020.9144899.

[79] J. Druant, T. Vyncke, F. De Belie, P. Sergeant, and J. Melkebeek, "Adding Inverter Fault Detection to Model-Based Predictive Control for Flying-Capacitor Inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2054–2063, 2015, doi: 10.1109/TIE.2014.2354591.

[80] L. Souto, J. Melendez, and S. Herraiz, "Fault Location in Power Distribution Networks using Arbitrary Similarity Criteria in the Principal Component Subspace," *2020 8th Int. Conf. Smart Energy Grid Eng. SEGE 2020*, pp. 92–96, 2020, doi: 10.1109/SEGE49949.2020.9182029.

[81] T. Wang, H. Xu, J. Han, E. Elbouchikhi, and M. E. H. Benbouzid, "Cascaded H-Bridge Multilevel Inverter System Fault Diagnosis Using a PCA and Multiclass Relevance Vector Machine Approach," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7006–7018, 2015, doi: 10.1109/TPEL.2015.2393373.

[82] S. Yin, S. X. Ding, P. Zhang, A. Hagahni, and A. Naik, *Study on modifications of PLS approach for process monitoring*, vol. 44, no. 1 PART 1. IFAC, 2011.

[83] M. Kumar, "Open Circuit Fault Detection and Switch Identification for LS-PWM H-Bridge Inverter," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 68, no. 4, pp. 1363–1367, 2021, doi: 10.1109/TCSII.2020.3035241.

[84] H. Truong, C. Mai, C. Nguyen, and P. Vu, "Modified space vector modulation for cascaded H-bridge multilevel inverter with open-circuit power cells," *J. Electr. Comput. Eng.*, vol. 2021, 2021, doi: 10.1155/2021/6643589.

[85] K. Sarita, S. Member, S. Kumar, S. Member, R. K. Saket, and S. Member, "Open-Circuit Fault Diagnosis in Multilevel Inverters Implementing PCA-WE-SVM Technique," *IEEE Trans. Ind. Appl.*, no. September, 2020.

[86] F. Charfi, F. Sellami, and K. Al-Haddad, "Fault diagnostic in power system using wavelet transforms and neural networks," *IEEE Int. Symp. Ind. Electron.*, vol. 2, no. 1, pp. 1143–1148, 2006, doi: 10.1109/ISIE.2006.295798.

[87] V. Vinothkumar and C. Muniraj, "Fault diagnosis in diode clamped multilevel inverter drive using wavelet transforms," *2013 Int. Conf. Green High Perform. Comput. ICGHPC 2013*, pp. 1–6, 2013, doi: 10.1109/ICGHPC.2013.6533925.

[88] A. Anand, N. Raj, S. George, and G. Jagadanand, "Wavelet-based open switch fault diagnosis in cascaded H-bridge multilevel inverter-fed induction motor drive," *IEEE Reg. 10 Annu. Int. Conf. Proceedings/TENCON*, vol. 2017-Decem, pp. 545–550, 2017, doi: 10.1109/TENCON.2017.8227923.

[89] R. G. Carvajal, J. Galan, and A. Torralba, "Wavelet neural network approach for fault diagnosis of analogue circuits," *IEE Proc.-Circuits Devices Syst.*, vol. 152, no. 5, pp. 379–385, 2005, doi: 10.1049/ip-cds.

[90] S. Liu, X. Qian, H. Wan, Z. Ye, S. Wu, and X. Ren, "NPC Three-level inverter open-circuit fault diagnosis based on adaptive electrical period partition and random forest," *J. Sensors*, vol. 2020, 2020, doi: 10.1155/2020/9206579.

[91] H. T. A.kelati, H.gaber, J.plosila, "Implementation of K-nearest Neighbor on Field Programmable Gate Arrays for Appliance Classification," *2020 8th Int. Conf. Smart Energy Grid Eng. SEGE 2020*, pp. 51–57, 2020, doi: 10.1109/SEGE49949.2020.9181975.

[92] K. K. I.Yaichi, A.Harrouz, I.Boussaid, A.Semmah, P.Wira, I.Colak, "An improved DTC strategy for a DFIG using an artificial neural network controller," *9th Int. Conf. Smart Grid, icSmartGrid 2021*, pp. 231–237, 2021, doi: 10.1109/icSmartGrid52357.2021.9551251.

[93] M. Colak and S. Balci, "Intelligent techniques to connect renewable energy sources to the grid: A review," *9th Int. Conf. Smart Grid, icSmartGrid 2021*, pp. 179–185, 2021, doi: 10.1109/icSmartGrid52357.2021.9551224.

[94] A. H. E. A.Sallam, Ragi.A.R, Hamdy, M.Z.Moustafa, "New measurement technique for modular multilevel converter with IGBT open-circuit failure detection and tolerance control for three-level submodule," vol. 5, pp. 1–6, 2016.

[95] Y. L. Murphey, M. A. Masrur, Z. H. Chen, and B. Zhang, "Model-based fault diagnosis in electric drives using machine learning," *IEEE/ASME Trans. Mechatronics*, vol. 11, no. 3, pp. 290–303, 2006, doi: 10.1109/TMECH.2006.875568.

[96] R. B. A.Benyamina, S. Moulahoum, I.Colak, "Hybrid fuzzy logic-artificial neural network controller for shunt active power filter," *2016 IEEE Int. Conf. Renew. Energy Res. Appl. ICRERA 2016*, vol. 5, pp. 837–844, 2017, doi: 10.1109/ICRERA.2016.7884454.

[97] N. Raj, G. Jagadanand, and S. George, "Fault detection and diagnosis in asymmetric multilevel inverter using artificial neural network," *Int. J. Electron.*, vol. 105, no. 4, pp. 559–571, 2018, doi: 10.1080/00207217.2017.1378382.

[98] S. Khomfoi and L. M. Tolbert, "Fault detection and reconfiguration technique for cascaded H-bridge 11-level inverter drives operating under faulty condition," *Proc. Int. Conf. Power Electron. Drive Syst.*, pp. 1035–1042, 2007, doi: 10.1109/PEDS.2007.4487831.

[99] A. Chappa, S. Gupta, L. K. Sahu, and K. K. Gupta, "Fault Diagnosis of Cascaded H-bridge Multilevel Inverter by DWPT Multi resolution and ANN," *2020 1st Int. Conf. Power, Control Comput. Technol. ICPC2T 2020*, pp. 128–133, 2020, doi: 10.1109/ICPC2T48082.2020.9071512.

[100] P. Achintya and L. Kumar Sahu, "Open circuit switch fault detection in multilevel inverter topology using machine learning techniques," *PIICON 2020 - 9th IEEE Power India Int. Conf.*, 2020, doi: 10.1109/PIICON49524.2020.9112870.

[101] E. Parimalasundar and N. Suthanthira Vanitha,

"Identification of open-switch and short-switch failure of multilevel inverters through DWT and ANN approach using LabVIEW," *J. Electr. Eng. Technol.*, vol. 10, no. 6, pp. 2277–2287, 2015, doi: 10.5370/JEET.2015.10.6.2277.

[102] T. Wang, J. Qi, H. Xu, Y. Wang, L. Liu, and D. Gao, "Fault diagnosis method based on FFT-RPCA-SVM for Cascaded-Multilevel Inverter," *ISA Trans.*, vol. 60, pp. 156–163, 2016, doi: 10.1016/j.isatra.2015.11.018.

[103] D. Chowdhury, M. Bhattacharya, D. Khan, S. Saha, and A. Dasgupta, "Wavelet decomposition based fault detection in cascaded H-bridge multilevel inverter using artificial neural network," *RTEICT 2017 - 2nd IEEE Int. Conf. Recent Trends Electron. Inf. Commun. Technol. Proc.*, vol. 2018-Janua, pp. 1931–1935, 2017, doi: 10.1109/RTEICT.2017.8256934.

[104] T. G. Manjunath and A. Kusagur, "Multilevel inverter fault diagnosis using optimised radial basis neural network - A novel performance enhancement," *2016 Int. Conf. Electr. Electron. Commun. Comput. Optim. Tech. ICEECCOT 2016*, pp. 102–105, 2017, doi: 10.1109/ICEECCOT.2016.7955194.

[105] R. Ramkumar, R. Harine, G. Akthar Shehanaz, S. Gowthami, and A. Professor, "Fault Detection and Diagnosition System for a 19 Level Cascaded Multilevel Inverter using ANN," *Int. J. Sci. Res. Sci. Technol.*, vol. 7, no. 3, pp. 153–159, 2017.

[106] R. Rajabioun, "Cuckoo optimization algorithm," *Appl. Soft Comput. J.*, vol. 11, no. 8, pp. 5508–5518, 2011, doi: 10.1016/j.asoc.2011.05.008.

[107] T. G. and A. Kusagur, "Robust Fault Detection of Multilevel Inverter using Optimized Radial Basis Function based Artificial Neural Network in Renewable Energy Power Generation Application," *Int. J. Comput. Appl.*, vol. 180, no. 48, pp. 8–15, 2018, doi: 10.5120/ijca2018917231.

[108] H. Benbouhenni and O. Maurice, "Utilization of an ANFIS-STSM Algorithm to Minimize Total Harmonic Distortion," *Int. J. Smartgrid*, vol. 4, no. 2, 2020.

[109] C. N. Ibem, M. E. Farrag, and A. A. Aboushady, "New Fuzzy Logic Based Switch-Fault Diagnosis in Three Phase Inverters," *UPEC 2020 - 2020 55th Int. Univ. Power Eng. Conf. Proc.*, 2020, doi: 10.1109/UPEC49904.2020.9209873.

[110] N. V. P. Kuraku, Y. He, T. Shi, R. K. Gatla, and R. Yi, "Fuzzy logic based open-circuit fault diagnosis in IGBT for CMLI fed PMSM drive," *Microelectron. Reliab.*, vol. 100–101, no. May, p. 113415, 2019, doi: 10.1016/j.microrel.2019.113415.

[111] M. Aly and H. Rezk, "An Efficient Fuzzy Logic Fault Detection and Identification Method of Photovoltaic Inverters," *Comput. Mater. Contin.*, vol. 67, no. 2, pp. 2283–2299, 2021, doi: 10.32604/cmc.2021.014786.

[112] J. Xu, B. Song, J. Zhang, and L. Xu, "A new approach to fault diagnosis of multilevel inverter," *Proc. 30th Chinese Control Decis. Conf. CCDC 2018*, pp. 1054–1058, 2018, doi: 10.1109/CCDC.2018.8407285.

[113] C. Huang, J. Zhao, and C. Wu, "Data-based inverter IGBT open-circuit fault diagnosis in vector control induction motor drives," *Proc. 2013 IEEE 8th Conf. Ind. Electron. Appl. ICIEA 2013*, pp. 1039–1044, 2013, doi: 10.1109/ICIEA.2013.6566520.

[114] A. Belaout, F. Krim, A. Mellit, B. Talbi, and A. Arabi, "Multiclass adaptive neuro-fuzzy classifier and feature selection techniques for photovoltaic array fault detection and classification," *Renew. Energy*, vol. 127, pp. 548–558, 2018, doi: 10.1016/j.renene.2018.05.008.

[115] V. Devadoss, P. Chandramohanan, and H. Al, "Diagnosis of Faulty IGBT Switches in Multi-Level Inverter Using ANFIS Technique," *Turkish J. Comput. Math. Educ.*, vol. 12, no. 6, pp. 5626–5634, 2021.

[116] H. Hu, F. Feng, and T. Wang, "Open-circuit fault diagnosis of NPC inverter IGBT based on independent component analysis and neural network," *Energy Reports*, vol. 6, pp. 134–143, 2020, doi: 10.1016/j.egyr.2020.11.273.

[117] L. Kou, C. Liu, G. wei Cai, and Z. Zhang, "Fault Diagnosis for Power Electronics Converters based on Deep Feedforward Network and Wavelet Compression," *Electr. Power Syst. Res.*, vol. 185, no. August 2018, p. 106370, 2020, doi: 10.1016/j.epsr.2020.106370.

[118] W. Jiang, C. Wang, Y. P. Li, and M. Wang, "Fault detection and remedy of multilevel inverter based on BP neural network," *Asia-Pacific Power Energy Eng. Conf. APPEEC*, vol. 1, pp. 2–5, 2012, doi: 10.1109/APPEEC.2012.6307658.

[119] S. K. M.Hallouz, N.Kabache, S.Moulahoum, "Neural Network Based Field Oriented Control for Doubly-Fed Induction Generator," *Int. J. Smart Grid - ijSmartGrid*, vol. 2, no. 3, pp. 183–187, 2018.

[120] G. K. Kumar, E. Parimalasundar, D. Elangovan, P. Sanjeevikumar, F. Lannuzzo, and J. B. Holm-Nielsen, "Fault investigation in cascaded H-bridge multilevel inverter through fast fourier transform and artificial neural network approach," *Energies*, vol. 13, no. 6, 2020, doi: 10.3390/en13061299.

[121] M. Sivakumar and R. M. S. Parvathi, "Particle swarm and neural network approach for fault clearing of multilevel inverters," *Am. J. Appl. Sci.*, vol. 10, no. 6, pp. 579–595, 2013, doi: 10.3844/ajassp.2013.579.595.

[122] S. S. Moosavi, A. Djerdir, Y. Ait-Amirat, D. A. Khaburi, and A. N'Diaye, "Artificial neural network-based fault diagnosis in the AC-DC converter of the power supply of series hybrid electric vehicle," *IET Electr. Syst. Transp.*, vol. 6, no. 2, pp. 96–106, 2016, doi: 10.1049/iet-est.2014.0055.

[123] S. P. Gautam, L. Kumar, S. Gupta, and N. Agrawal, "A Single-Phase Five-Level Inverter Topology with Switch Fault-Tolerance Capabilities," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2004–2014, 2017, doi: 10.1109/TIE.2016.2626368.

[124] C. Sadanala, S. Pattnaik, and V. P. Singh, "Fault

tolerant architecture of an efficient five-level multilevel inverter with overload capability characteristics," *IET Power Electron.*, vol. 13, no. 2, pp. 368–376, 2020, doi: 10.1049/iet-pel.2019.0736.

[125] M. R. A and K. Sivakumar, "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7569–7577, 2015, doi: 10.1109/TIE.2015.2455523.

[126] S. Ceballos, J. Pou, J. Zaragoza, E. Robles, J. L. Villate, and J. L. Martín, "Fault-tolerant neutral-point-clamped converter solutions based on including a fourth resonant leg," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2293–2303, 2011, doi: 10.1109/TIE.2010.2069075.

[127] M. Aly, E. M. Ahmed, and M. Shoyama, "A New Single-Phase Five-Level Inverter Topology for Single and Multiple Switches Fault Tolerance," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9198–9208, 2018, doi: 10.1109/TPEL.2018.2792146.

[128] M. Jalhotra, S. P. Gautam, L. Kumar, S. Gupta, and A. Hema Chander, "Fault tolerance and energy sharing analysis of a single phase multilevel inverter topology," *Proc. IECON 2018 - 44th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 1209–1213, 2018, doi: 10.1109/IECON.2018.8591853.

[129] A. Chappa, S. Gupta, L. K. Sahu, and K. K. Gupta, "A Fault-Tolerant Multilevel Inverter Topology with Preserved Output Power and Voltage Levels under Pre-And Postfault Operation," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5756–5764, 2021, doi: 10.1109/TIE.2020.2994880.

[130] R. Jun Li, Jing Xu, Lisa Qi, Zach Pan, Burgos, V. Tech, and A. F. A. Inverters, "Analysis and Control of Fault Tolerant Operation of Five level ANPC Inverters," *Ieee Work. COMPEL*, pp. 1–6, 2014.

[131] Y. J. Kim, S. H. Kim, S. M. Kim, and K. B. Lee, "Open Fault Diagnosis and Tolerance Control for Grid-Connected Hybrid Active Neutral-Point-Clamped Inverters with Optimized Carrier-Based Pulse Width Modulation," *IEEE Access*, vol. 8, pp. 145542–145551, 2020, doi: 10.1109/ACCESS.2020.3013566.

[132] P. Azer, S. Ouni, and M. Narimani, "A Novel Fault-Tolerant Technique for Active-Neutral-Point-Clamped Inverter Using Carrier-Based PWM," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 1792–1803, 2020, doi: 10.1109/TIE.2019.2903764.

[133] L. M. Halabi, I. M. Alsofyani, and K. B. Lee, "Multiple-fault-Tolerant strategy for three-phase hybrid active neutral point clamped converters using enhanced space vector modulation technique," *IEEE Access*, vol. 8, pp. 180113–180123, 2020, doi: 10.1109/ACCESS.2020.3028115.

[134] H. Wang, "A Short-Circuit Fault-Tolerant Strategy for Three- Phase Four-Wire Flying Capacitor Three-Level Inverters," *IEEE 10th Int. Symp. Power Electron. Distrib. Gener. Syst.*, no. 51777189, pp. 781–786, 2019, doi: 10.1109/PEDG.2019.8807759.

[135] X. Kou, K. A. Corzine, and Y. L. Familiant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 979–987, 2004, doi: 10.1109/TPEL.2004.830037.

[136] R. P. Aguilera, D. E. Quevedo, T. J. Summers, and P. Lezana, "Predictive control algorithm robustness for achieving fault tolerance in multicell converters," *IECON Proc. (Industrial Electron. Conf.*, pp. 3302–3308, 2008, doi: 10.1109/IECON.2008.4758489.

[137] J. Amini and M. Moallem, "A Fault-Diagnosis and Fault-Tolerant Control Scheme for Flying Capacitor Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 1818–1826, 2017, doi: 10.1109/TIE.2016.2624722.

[138] A. Chen, C. Zhang, X. He, and N. Cui, "Fault-tolerant design for flying capacitor multilevel inverters," *2009 IEEE 6th Int. Power Electron. Motion Control Conf. IPEMC '09*, vol. 3, pp. 1460–1464, 2009, doi: 10.1109/IPEMC.2009.5157616.

[139] S. K. Maddugari, V. B. Borghate, and S. Member, "A Reliable Fault Tolerant Inverter," *IEEE Conf. Proc.*, pp. 2–6, 2020, doi: 10.1109/stpec49749.2020.9297681.

[140] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan, and M. Abapour, "Fault-tolerant structure for cascaded h-bridge multilevel inverter and reliability evaluation," *IET Power Electron.*, vol. 10, no. 1, pp. 59–70, 2017, doi: 10.1049/iet-pel.2015.1025.

[141] H. K. Jahan, F. Panahandeh, M. Abapour, and S. Tohidi, "Reconfigurable Multilevel Inverter with Fault-Tolerant Ability," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7880–7893, 2018, doi: 10.1109/TPEL.2017.2773611.

[142] A. A. Stonier and B. Lehman, "An Intelligent-Based Fault-Tolerant System for Solar-Fed Cascaded Multilevel Inverters," *IEEE Trans. Energy Convers.*, vol. 33, no. 3, pp. 1047–1057, 2018, doi: 10.1109/TEC.2017.2786299.

[143] H. Salimian and H. Iman-Eini, "Fault-Tolerant Operation of Three-Phase Cascaded H-Bridge Converters Using an Auxiliary Module," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1018–1027, 2017, doi: 10.1109/TIE.2016.2613983.

[144] V. S. P. K, S. Peddapati, and S. Naresh, "A New Fault-Tolerant MLI - Investigating Its Skipped Level Performance," *IEEE Trans. Ind. Electron.*, vol. 0046, no. c, 2021, doi: 10.1109/TIE.2021.3062259.

[145] N. K. Dewangan, T. K. Tailor, R. Agrawal, P. Bhatnagar, and K. K. Gupta, "A multilevel inverter structure with open circuit fault-tolerant capability," *Electr. Eng.*, no. 0123456789, 2021, doi: 10.1007/s00202-020-01149-6.

[146] S. M. Kim, J. S. Lee, and K. B. Lee, "A Modified Level-Shifted PWM Strategy for Fault-Tolerant Cascaded Multilevel Inverters with Improved Power Distribution," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7264–7274, 2016, doi: 10.1109/TIE.2016.2547917.

[147] L. Xiong, F. Zhuo, X. Liu, Z. Xu, and Y. Zhu, "Fault-Tolerant Control of CPS-PWM-Based Cascaded Multilevel Inverter with Faulty Units," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 4, pp. 2486–2497, 2019, doi: 10.1109/JESTPE.2019.2898907.

[148] T. Wang, J. Zhang, H. Wang, Y. Wang, D. Diallo, and M. Benbouzid, "Multi-mode fault-tolerant control strategy for cascaded H-bridge multilevel inverters," *IET Power Electron.*, vol. 13, no. 14, pp. 3119–3126, 2020, doi: 10.1049/iet-pel.2020.0109.

[149] A. T. S.Benanti, C.Buccella, M.Caruso, V.castiglia, C.Cecati, "Experimental analysis with FPGA controller-based of MC PWM techniques for three-phase five level cascaded H-bridge for PV applications," *IEEE Int. Conf. Renew. Energy Res.*, vol. 5, pp. 1173–1178, 2016, doi: 10.1109/ICRERA.2016.7884518.

[150] M. Jalhotra, L. K. Sahu, S. Gupta, and S. P. Gautam, "Resilient Fault-Tolerant Topology of Single-Phase Multilevel Inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 2, pp. 1915–1922, 2021, doi: 10.1109/JESTPE.2019.2936271.

[151] T. J. Nistane, L. K. Sahu, M. Jalhotra, and S. P. Gautam, "Single and multiple switch fault-tolerance capabilities in a hybrid five-level inverter topology," *IET Power Electron.*, vol. 13, no. 6, pp. 1257–1266, 2020, doi: 10.1049/iet-pel.2019.0716.

[152] S. P. Gautam, S. Gupta, and L. Kumar, "Reliability improvement of transistor clamped H-bridge-based cascaded multilevel inverter," *IET Power Electron. Res.*, pp. 770–781, 2017, doi: 10.1049/iet-pel.2016.0574.

[153] B. S. Kumar and A. Kirubakaran, "A Complete Fault-Tolerant Solution for A Single-Phase Five-Level Hybrid Flying Capacitor Inverter," *2019 Innov. Power Adv. Comput. Technol. i-PACT 2019*, pp. 1–5, 2019, doi: 10.1109/i-PACT44901.2019.8960006.

[154] R. Choupan, S. Golshannavaz, D. Nazarpour, and M. Barmala, "A new structure for multilevel inverters with fault-tolerant capability against open circuit faults," *Electr. Power Syst. Res.*, vol. 168, no. November 2018, pp. 105–116, 2019, doi: 10.1016/j.epsr.2018.11.013.

[155] N. K. Dewangan, P. Bhatnagar, S. K. Jain, S. Gupta, and K. K. Gupta, "Open-Switch Fault Tolerance Capabilities of Some Reduced Device Count Multilevel Inverter Topologies," *Iran. J. Sci. Technol. - Trans. Electr. Eng.*, vol. 44, no. 1, pp. 253–264, 2020, doi: 10.1007/s40998-019-00241-3.

[156] M. Santosh Kumar, V. B. Borghate, and S. Sabyasachi, "A Generalized Fault Tolerant Multilevel Inverter for Switch Open-Circuit Faults," *Proc. 2018 IEEE Int. Conf. Power Electron. Drives Energy Syst. PEDES 2018*, pp. 1–6, 2018, doi: 10.1109/PEDES.2018.8707742.

[157] S. Sabyasachi, V. B. Borghate, S. K. Maddugari, and R. R. Karasani, "A reliable multilevel inverter with fault tolerance," *IEEE Reg. 10 Annu. Int. Conf. Proceedings/TENCON*, vol. 2017-Decem, pp. 557–562, 2017, doi: 10.1109/TENCON.2017.8227925.

[158] M. M. Rahman, S. Hossain, and S. Rezwan, "Seven-Level Cascaded H-Bridge Inverter and Fault-Tolerant Control Strategy," *ICIET 2019 - 2nd Int. Conf. Innov. Eng. Technol.*, vol. 3, no. 1, pp. 23–24, 2019, doi: 10.1109/ICIET48527.2019.9290714.

[159] Manik, S. P. Gautam, L. Kumar, A. Hema Chander, and S. Gupta, "Reliability analysis of a novel fault tolerant multilevel inverter topology," *Proc. IECON 2018 - 44th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 1460–1465, 2018, doi: 10.1109/IECON.2018.8592684.

[160] A. M. Youssef, "Multiphase Interleaved Bidirectional DC/DC Converter for Fuel Cell/Battery Powered Electric Vehicles," *2020 12th Int. Conf. Electr. Eng. ICEENG 2020*, vol. 4, no. 2, pp. 34–43, 2020, doi: 10.1109/ICEENG45378.2020.9171753.

[161] M. A. Zdiri, B. Khelifi, F. Ben Salem, and H. H. Abdallah, "A Comparative Study of Distinct Advanced MPPT Algorithms for a PV Boost Converter," *Int. J. Renew. Energy Res.*, vol. 11, no. 3, pp. 1156–1164, 2021.

[162] D. S. Pillai and N. Rajasekar, "A comprehensive review on protection challenges and fault diagnosis in PV systems," *Renew. Sustain. Energy Rev.*, vol. 91, no. March, pp. 18–40, 2018, doi: 10.1016/j.rser.2018.03.082.

[163] H. Mekki, A. Mellit, and H. Salhi, "Artificial neural network-based modelling and fault detection of partial shaded photovoltaic modules," *Simul. Model. Pract. Theory*, vol. 67, pp. 1–13, 2016, doi: 10.1016/j.simpat.2016.05.005.

[164] K. Nallamekala, S. Dandabatthina, and V. K. Tella, "A novel fault tolerant 21-level inverter configuration for PV applications," *Proc. IEEE Int. Conf. Circuit, Power Comput. Technol.*, 2017, doi: 10.1109/ICCPCT.2017.8074239.

[165] K. Roopa, P. Jugge, and S. T. Kalyani, "A new 15-level inverter configuration with fault tolerant capability for PV applications," *IEEE Int. Conf. Power, Control. Signals Instrum. Eng. ICPCSI 2017*, pp. 1830–1835, 2018, doi: 10.1109/ICPCSI.2017.8392031.

[166] M. N. Rao, N. Karthick, and A. M. Rao, "Fault tolerant ability of a multi level inverter fed three phase induction motor for water pumping application," *Proc. 7th Int. Conf. Electr. Energy Syst. ICEES 2021*, pp. 212–216, 2021.

[167] Z. Liu, S. Wang, Z. Ji, X. Ji, and Y. Xie, "A novel fault-tolerant control for battery-energy-storage system based on cascaded multilevel converter with battery/BMS failure," *Microelectron. Reliab.*, vol. 88–90, no. June, pp. 1268–1273, 2018, doi: 10.1016/j.microrel.2018.06.067.