Design and Analysis of Enhanced Boost Active Switch Controlled Based ZSI for Photovoltaic DG System

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Abstract- This paper introduces a new topology for the applications in single stage photovoltaic distributed generation (PVDG) system. The proposed topology is named as Enhanced boost active switch controlled based Z-source Inverter (EBASC-ZSI). The EBASC-ZSI is capable of boosting the output voltage coming from photovoltaic panel with low value of shoot through state duty cycle (D). The EBASC-ZSI is compared with some of the topologies in the field of ZSI name as qZS, DA-qZSI and CA-qZSI. The EBASC-ZSI topology provides higher boosting voltage than DA-qZSI and qZS topology but similar boosting voltage like CA-qZSI topology at lower value of D. The EBASC-ZSI topology used a less pair of LC components but used one more switch in comparison to CA-qZSI. While in comparison to DA-qZSI topology, it has used a less inductor, an additional capacitor, same number of diodes and an additional switch in the Z-impedance. The capacitor voltage stress of EBASC-ZSI increases initially in comparison to CA-qZSI but decreases thereafter as the value of D increases. The current stress through one inductor of EBASC-ZSI is same in comparison to CA-qZSI and DA-qZSI. While the current stress through another inductor of EBASC-ZSI is less in comparison to CA-qZSI and DA-qZSI. The Simulink model and the hardware prototype of the topology has developed in the laboratory and presented in this paper.
Keywords Boosting topology, Z-source inverter, single stage, photovoltaic, current stress.

1. Introduction

In the traditional voltage source inverter [1], the maximum output voltage obtained from the ac side was depending upon the magnitude of dc input voltage provided to the inverter. As a consequence, the output voltage of the inverter cannot be increases according to the need of the load.

Hence to address the above shortcomings, the buck/boost converter was used [2]. The buck/boost converter is an additional circuit between the input dc voltage and inverter and is capable to vary the input voltage to the inverter according to the need of the load. However, using of additional circuits between the input voltage and the inverter made the circuits to double stage where one stage do the work of buck/boost and another stage does the conversion of dc into ac waveform. No doubt, the circuit solves one problem regarding buck/boost voltage to the inverter. However it creates several problems like system complexity and reduction of efficiency by increasing the losses. Moreover it creates the space to develop further system which can boost the voltage more in comparison to above described system.

As the output of the photovoltaic (PV) panel is dc in nature and has generally a lower value, there is a need to boost the voltage to the inverter from the PV panel to meet the demand of the load. However the limited voltage boosting ability of the boost converter along with the drawbacks of the double stage system limited its choice for applications in solar PVDG system. Hence it forced to go for finding a better alternative for boosting the voltage of PV panel.

The above drawbacks for boosting the voltage of dc source has been addressed by the topology introduced in [3,4]. The topology is known as Z-source inverter (ZSI). The ZSI boosted the input voltage coming from the DC-source or PV panel more as compared to boost converter and also in a single stage system. However the drawbacks of the ZSI like

discontinuous input current and more stress on its components made its applications limited.

Moving ahead for the development of new topologies for the applications in PV panel or dc source, a topology proposed in [5] known as quasi Z-source inverter (qZSI). The qZSI provides same voltage gain in comparison to ZSI but it removes several drawbacks of ZSI like discontinuous input current from the source and high stress on the components used in the impedance in the ZSI. The qZSI then widely used in single stage solar PVDG system.

Moving further, a topology developed in [6] known as switch boost inverter (SBI). It provides same boosting factor as that of ZSI and qZSI topologies while using less components in its Z-network comparing ZSI and qZSI. But its application is limited where the power input is low.

Again to improve the boosting capabilities of ZSI, two new topologies proposed in [7]. The topologies are known as capacitor assisted quasi Z-source inverter (CA-qZSI) and diode assisted quasi Z-source inverter (DA-qZSI). The topologies provide more voltage boosting in comparison to ZSI and qZSI, but it used more number of components in its Z-network which made the system bulky. Also the efficiency decreases due to increase the losses in its components.

In further succession to increase the gain of ZSI and qZSI topologies, a concept known as switch inductor was introduced. The SL consists of two inductor and three diodes. The SL then applied in ZSI [8] and qZSI [9] known as SL-ZSI and SL-qZSI. After the application of SL in ZSI and qZSI, the voltage boosting capabilities of ZSI and qZSI increases. However, due to more inductors and diodes in the Z-network of SL-ZSI and SL-qZSI the losses increases, thereby reducing the efficiency.

In this manuscript a new topology is proposed for the applications of single stage PVDG system and is named as EBASC-ZSI. The EBASC-ZSI provides more voltage gain in comparison to ZSI, qZSI, DA-qZSI and SBI at same value of D. While in comparison with CA-qZSI, it provides similar voltage gain at a lower value of D. The topology mathematical modeling, simulink modeling and hardware prototype has been matched and is described in the below section.

The manuscript has divided into different section. The description of double stage and single stage system has explained in section 2. The topology operation principle is described in section 3. The comparison of EBASC-ZSI topology with some of the existing topologies is described in section 4. The EBASC-ZSI topology simulation results is described in section 5. The experimental results of EBASC-ZSI is described in section 6. Finally the conclusion of the research work is described in section 7.

2. Double Stage and Single Stage PVDG System

2.1. Double Stage PVDG System

From Fig. 1, the double stage PVDG system is made up of a PV panel followed by a boost converter and then an inverterfollowed with the grid. The PV panel output power is pass through boost converter. The MPPT controller provides the duty cycle to the boost converter. The boost converter then increased the dc-link voltage to the inverter as per the requirement. The inverter just converts the dc-link voltage into output ac-voltage. As an additional stage is required to provide input voltage to the inverter, hence it is known as double stage PVDG system. In addition to the above the dc-dc boost converter can be used to provide multiple output from hybrid energy systems [10]. However, the dc-dc boost converter can provide the dc-power only unlike a single converter in [11], which provides both dc-power and ac-power and can be used for multiple purposes.

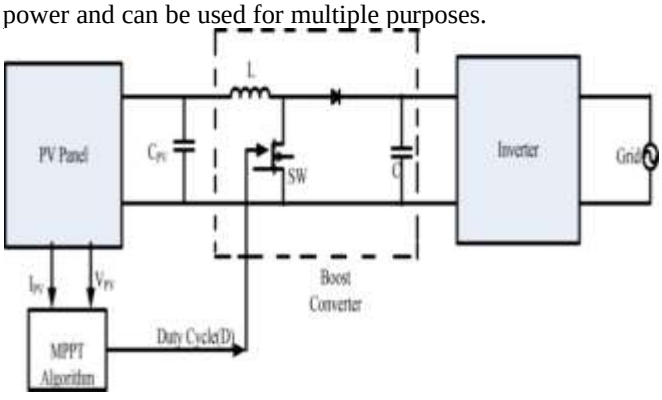


Fig. 1. Double stage PVDG system

2.2. Single Stage PVDG System

Fig. 2 shows the example of a single stage PVDG system. In single stage PVDG system, the input to the inverter comes from the PV panel. Unlike in double stage PVDG system, where the voltage input to the inverter comes

from a boost converter. However, when the voltage requirement of the AC side is high, then the inverter is replaced by ZSI/qZSI [4,5]. The boosting capability of qZSI is more than that of boost converter at the same value of D. However, when the voltage boosting is more required at the same value of D, then another topology is required in place of qZSI. In this paper a new EBASC-ZSI topology is introduced and can serve the purpose more than qZSI (due to its more voltage boosting factor). The EBASC-ZSI topology can be applied in a single stage PVDG system.

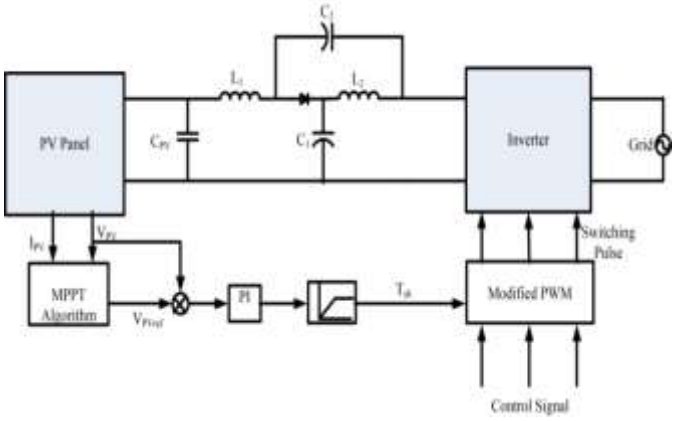


Fig. 2. Single stage PVDG system

2.3. Maximum Power Point Tracking (MPPT) Controller

The MPPT controller is required in case of both the double stage PVDG system and the single stage PVDG system [12,13]. The work of MPPT controller is to find the voltage corresponding to maximum power in the power verses voltage curve. From tracking the maximum voltage, it provides the duty cycle as the output or reference voltage. However in case of double stage PVDG system, the MPPT controller provides the duty cycle to the boost converter. In case of single stage PVDG system the MPPT controller provides the reference value of maximum output PV panel voltage. The reference voltage is then compared with the actual voltage of the PV panel. Then the error signal is processed through controller to provide PWM control signal to the switches.

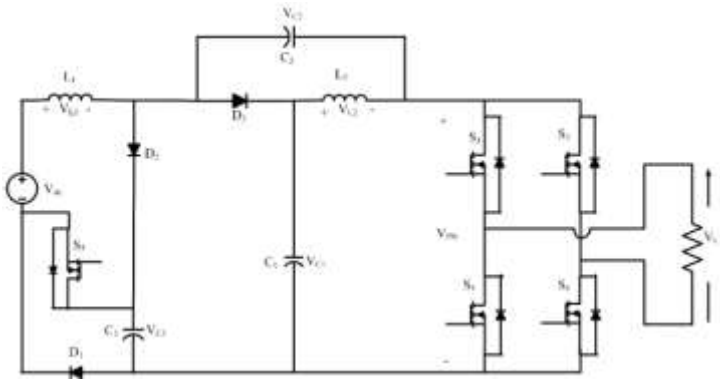


Fig. 3. Schematic diagram of EBASC-ZSI topology.

3. Proposed Topology EBASC-ZSI

The schematic diagram of EBASC-ZSI topology is shown in Fig. 3. The topology provides more voltage gain as compared to several existing topologies. The topology operation principle, boost factor derivation and the designing of inductor and capacitor is described below subsections.

2.4. Operation Principles of EBASC-ZSI

Fig. 3 shows the EBASC-ZSI topology which is made up of a dc-source, a Z-impedance network, an inverter and a load. The Z-impedance network contains two inductors, three capacitors, three diodes and an extra switch (S_5). The topology operates in two modes i.e. shoot through (ST) state mode and non-shoot through (NST) state mode. The two modes of operations are described below,

2.4.1. ST State Mode

In the ST state mode, the same switching pulse is provided to either one leg or two legs of the inverter to make it short circuited. In this state, the capacitors get discharges and the inductors store energy in it. The discharge of capacitors C_1, C_3led to the storage of energy through inductor L_1while the discharge of capacitors C_2led to the storage of energy through inductor L_2. In this state the return path for the current is provided by the extra switchS_5. All the three diodes in the Z-network remained off in this state. The operational diagram in the ST state mode of the EBASC-ZSI topology is shown in Fig. 4. From Fig. 4, the voltage across inductor $L_1$and $L_2$are,

$$V_{L1} = V_{dc} + V_{C2} + V_{C3} \quad (1)$$

$$V_{L2} = V_{C1} \quad (2)$$

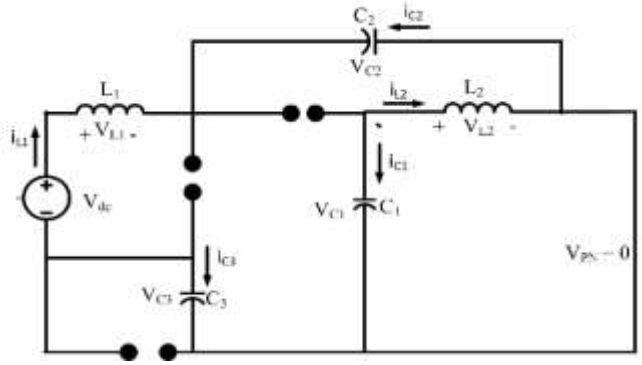


Fig. 4. Schematic diagram of EBASC-ZSI topology in ST state mode.

2.4.2. NST State Mode

In the NST state mode, the inductors discharge energy to the load while the capacitors get charged from the dc-source. In this state the EBASC-ZSI topology provides output power to the load unlike in ST state, where the output power to the load is zero. The normal operation of the inverter carried out in this state with the help of switching pulse to the switches. The inductors $L_1$and L_2 in this state releases their energy to the load while the capacitors C_1, C_2, C_3 gets charged through the DC-source. All the three diodes D_1, D_2 and D_3 remained on in this state. The extra switch S_5remained off in this state. The operational diagram of EBASC-ZSI topology in the NST state is shown in Fig. 5. From Fig. 5, the voltage across inductor L_1 and $L_2$are,

$$V_{L1} = V_{dc} - V_{C3} \tag{3}$$

$$V_{L1} = V_{dc} - V_{C1} \tag{4}$$

$$V_{L2} = -V_{C2} \tag{5}$$

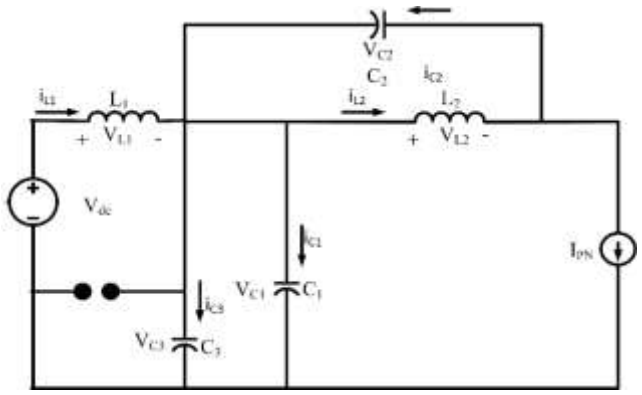


Fig. 5. Schematic diagram of EBASC-ZSI topology in NST state mode.

2.5. Stability Analysis

The stability analysis of EBASC-ZSI topology can be analyzed using state space matrix in both the ST state and NST state.

$$\frac{dx}{dt} = Ax + Bu \tag{6}$$

$$y = Cx + Du \tag{7}$$

Where A, B, C and D are state space, input, output and feed through matrices

2.5.1. The State Space Matrix in ST State

In ST state the matrix is

$$d/dt\begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} = \begin{bmatrix} \frac{r+2R}{L_1} & 0 & 0 & \frac{1}{L_1} & \frac{1}{L_2} \\ 0 & \frac{-(R+r)}{L_2} & \frac{1}{L_2} & 0 & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 & 0 \\ \frac{-1}{C_3} & 0 & 0 & 0 & 0 \\ \frac{-1}{C_3} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{dc} \\ I_{PN} \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} I_i \\ V_{PN} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{dc} \\ I_{PN} \end{bmatrix} \tag{9}$$

2.5.2. The state space matrix in NST state

In NST state the matrix is

$$d/dt\begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} = \begin{bmatrix} \frac{-(r+R/2)}{L_1} & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & \frac{-(R+r)}{L_2} & 0 & \frac{-1}{L_2} & 0 \\ \frac{1}{2C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 \\ \frac{1}{2C_3} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{R}{2L_1} \\ 0 & \frac{R}{L_2} \\ 0 & \frac{-1}{2C_1} \\ 0 & \frac{-1}{C_2} \\ 0 & \frac{-1}{2C_3} \end{bmatrix} \begin{bmatrix} V_{dc} \\ I_{PN} \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} I_i \\ V_{PN} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ R & R & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -2R \end{bmatrix} \begin{bmatrix} V_{dc} \\ I_{PN} \end{bmatrix} \tag{11}$$

Hence the average state space matrix from ST and NST state is given as

$$A = \begin{bmatrix} \frac{r(2D-1)+(R/2)(3D+1)}{L_1} & 0 & \frac{D-1}{L_1} & \frac{D}{L_1} & \frac{D}{L_2} \\ 0 & \frac{-(R+r)}{L_2} & \frac{D}{L_2} & \frac{D-1}{L_2} & 0 \\ \frac{1-D}{2C_1} & \frac{-D}{C_1} & 0 & 0 & 0 \\ \frac{-D}{C_3} & \frac{1-D}{C_2} & 0 & 0 & 0 \\ \frac{1-3D}{2C_3} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{12}$$

Hence by getting the getting the eigen values of the matrix A, the stability can be determined

2.6. Derivation of Boost Factor for EBASC-ZSI Topology

The Derivation of Boost Factor for the EBASC-ZSI topology is described below.

By applying Volt-Sec balance principle through inductor L_1,

$$D(V_{dc} + V_{C2} + V_{C3}) + (1-D)(V_{dc} - V_{C3}) = 0 \tag{13}$$

$$D(V_{dc} + V_{C2} + V_{C3}) + (1-D)(V_{dc} - V_{C1}) = 0 \tag{14}$$

Similarly, by applying Volt- Sec balance principle through inductor L_2,

$$D(V_{C1}) + (1-D)(-V_{C2}) = 0 \tag{15}$$

The voltage across capacitor C1, C2 and C3 can be find out from the Equation (13), (14) and (15),

$$V_{C1} = \frac{V_{dc}(1-D)}{1-3D+D^2} \tag{16}$$

$$V_{C2} = \frac{DV_{dc}}{1-3D+D^2} \tag{17}$$

$$V_{C3} = V_{C1} \tag{18}$$

The peak dc-link voltage is,

$$\hat{V}_{PN} = V_{C1} + V_{C2} = \frac{V_{dc}}{1-3D+D^2} \tag{19}$$

Hence the boost factor (B) of EBASC-ZSI topology given as,

$$B = \frac{\hat{V}_{PN}}{V_{dc}} = \frac{1}{1-3D+D^2} \tag{20}$$

2.7. PWM Switching Pulse Technique

The PWM switching pulse strategy for EBASC-ZSI topology have to modify in such a manner so as to accommodate the ST state duty cycle in it. Therefore the ST state duty cycle forms a part of the total switching state. In the EBASC-ZSI topology, the simple boost control technique [15] is used out of several PWM control strategy available for providing gate pulse to the switches of the ZSI [14-18].

2.8. Design of Inductor and Capacitor

The mathematical expression to find out the value of inductor and capacitor can be find out from the inductor current ripple and the capacitor currents in the ST state. From Equations (1), (2), (16), (17) and (18) the current ripple across inductor L_1 and L_2in ST state can be expressed as,

$$\Delta i_{L1} = \frac{(2-3D+D^2)D}{1-3D+D^2}\frac{V_{dc}}{L_1 K_{sh} f_s} \tag{21}$$

$$\Delta i_{L2} = \frac{D(1-D)}{1-3D+D^2}\frac{V_{dc}}{L_2 K_{sh} f_s} \tag{22}$$

Where K_{sh} is the number of times the ST period has been incorporated in a switching period.

Hence from Equation (21) and (22), the expressions of value of inductors are given as:

$$L_1 = \frac{(2-3D+D^2)D}{1-3D+D^2}\frac{V_{dc}}{\Delta i_{L1} K_{sh} f_s} \tag{23}$$

$$L_2 = \frac{D(1-D)}{1-3D+D^2}\frac{V_{dc}}{\Delta i_{L2} K_{sh} f_s} \tag{24}$$

The capacitor currents in ST state are given as:

$$i_{C1} = \frac{-(1-D)}{(1+D)(1-3D)} I_{PN} \tag{25}$$

$$i_{C2} = \frac{-(1-D)}{(1-3D)} I_{PN} \tag{26}$$

$$i_{C3} = \frac{-(1-D)}{(1-3D)} I_{PN} \tag{27}$$

From the Equations (25), (26) and (27) the capacitance value of different capacitors can be given as,

$$C_1 = \frac{D(1-D)}{(1+D)(1-3D)}\frac{I_{PN}}{\Delta V_{C1} K_{sh} f_s} \tag{28}$$

$$C_2 = \frac{D(1-D)}{(1-3D)}\frac{I_{PN}}{\Delta V_{C2} K_{sh} f_s} \tag{29}$$

$$C_3 = \frac{D(1-D)}{(1-3D)}\frac{I_{PN}}{\Delta V_{C3} K_{sh} f_s} \tag{30}$$

4. Comparison with Other Topologies

This part of the manuscript represents an elaborative comparison between the EBASC-ZSI topology with CA-qZSI, DA-qZSI and qZSI topologies. The topologies are compared with respect to topology characteristics, boost factor, voltage and current stress, number of components used in the Z-impedance.

2.9. Topology Characteristics Comparison

Table 1 shows the comparison of number of components used by EBASC-ZSI topology with respect to other topologies. Some good features of the proposed EBASC-ZSI topology over other topologies are (i) The boost factor is more than qZSI and DA-qZSI (ii) Inductor requirement is less in comparison to both DA-qZSI and CA-qZSI (iii) capacitor and diode requirement is less in comparison to CA-qZSI. However, it requires one additional active switch compared to other topologies.

2.10. Comparison of Voltage and Current Stress of Different Topologies

Considering the same input voltage to the Z-impedance of different topologies. The Table II shows the comparison with respect to boost factor (B), capacitor voltage stress (Vc/Vdc), diode voltage stress (VD/Vdc) and inductor current stress (IL/IPN) of different topologies.

Table 1. Comparison of inductors (L), capacitors (C), diodes (d)and extra switch (SW) used in the Z-impedance of different topologies

Name of the Component	Number of Components			
	qZSI	DA-qZSI	CA-qZSI	EBASC-ZSI
L	2	3	3	2
C	2	3	4	3
d	1	3	2	3
SW	0	0	0	1

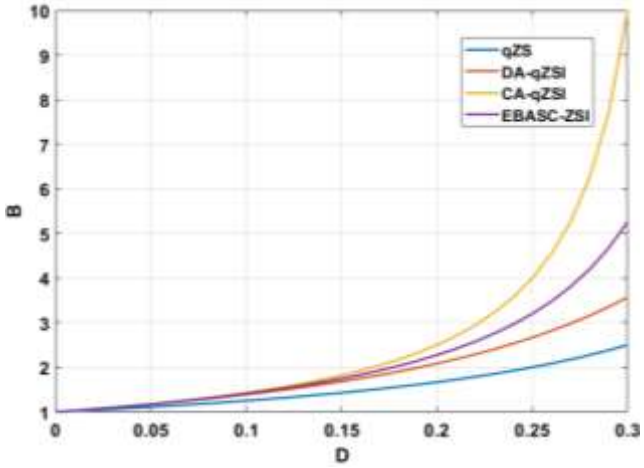
Table 2. Comparison of B, V_c/V_{dc}, V_D/V_{dc} and I_L/I_{PN} of different topologies

	qZS	DA-qZSI	CA-qZSI	EBASC-ZSI
Boost Factor (B)	1/(1-2D)	1/(1-D)(1-2D)	1/(1-3D)	1/(1-3D+D^2)
Capacitor Voltage Stresses (V_c/V_{dc})	(1-D)B DB	DB DB (1-2D)B	DB DB (1-2D)B DB	(1-D)B DB (1-D)B
Diode Voltage	B	B (1-2D)B	B B	(1-D)B B

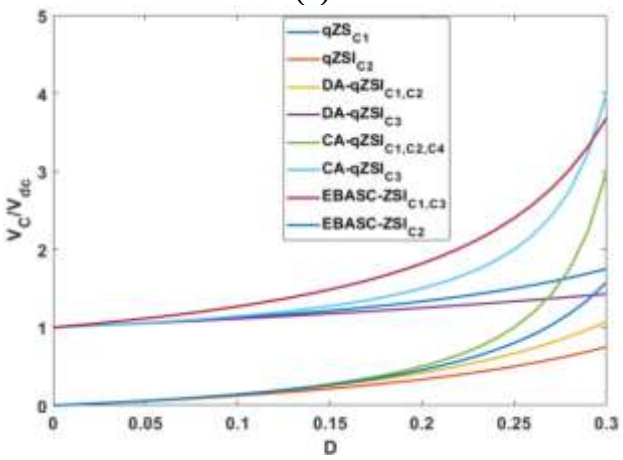
Stresses(V_D/V_{dc})		2DB		B
Inductor Current Stresses (I_L/I_{PN})	(1-D)/(1-2D) (1-D)/(1-2D)	(1-D)/(1-2D) (1-D)/(1-2D) (1-D)/(1-3D)	(1-D)/(1-3D) (1-D)/(1-3D) (1-D)/(1-3D)	(1-D)/(1-3D) (1-D)/(1+D)(1-3D)
Average dc-link Current (I_{PN})	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$

Where R_l is load resistance.

The graphical representation of comparison in Table 2 is shown below

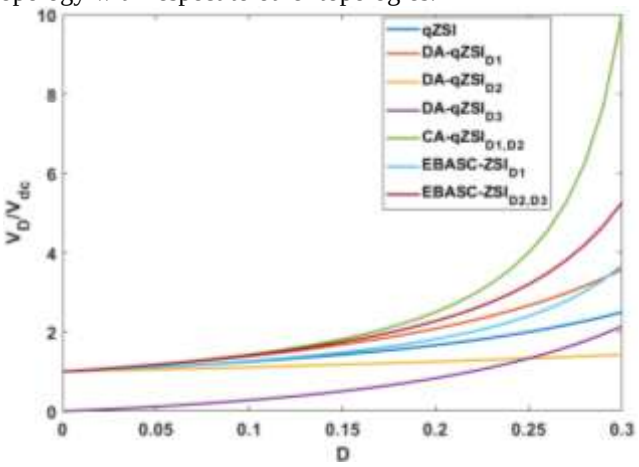


(a)

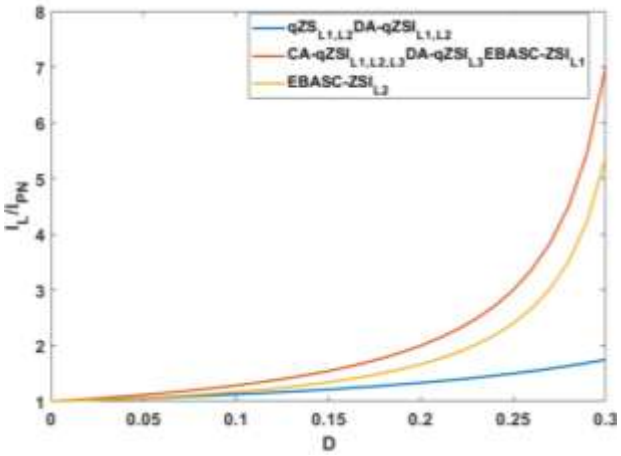


(b)

Fig. 6. (a) D vs Bcomparison of EBASC-ZSI with respect to other topologies (b) D vs V_c/V_{dc}comparison of EBASC-ZSI topology with respect to other topologies.



(a)



(b)

Fig. 7. (a) D vs V_d/V_{dc}compariosn of EBASC-ZSI topology with respect to other topologies (b) D vs IL/IPN comparison of EBASC-ZSI topology with reepect to other topologies.

From Fig. 6(a), it can be concluded that the boost factor of EBASC-ZSI is nearly same in comparison to CA-qZSI at lower value of D and higher with respect to other two topologies at all value of D. Fig. 6(b) shows that the voltage stress across some capacitor of EBASC-ZSI topology is less as compared to CA-qZSI, but in some other capacitors the voltage stress is higher than all the three compared topologies. Fig. 7(a) shows that the voltage stress across diode of EBASC-ZSI is higher in comparison to qZSI and DA-qZSI but lower than compared to CA-qZSI topology. Fig. 7(b) shows that the current stress through one inductor of EBASC-ZSI topology is same with all inductors of CA-qZSI. While current stress through another inductor of EBASC-ZSI, is less in comparison to CA-qZSI topology but higher than DA-qZSI topology.

2.11. Power Loss Calculation

The power loss in EBASC-ZSI is calculated after calculating the losses in the inductor, capacitor, diodes and in the switches of the inverter. The different losses calculation is described below.

2.11.1. Inductor Power Loss

Neglecting the winding core loss in the inductor due to its minimal value as compared to inductor copper loss. The inductor copper loss is calculated after multiplying the RMS current with its internal resistance (r_L). The inductors RMS current is given as,

$$I_{L1(RMS)} = \frac{1-D}{1-3D} I_{PN} \tag{31}$$

$$I_{L2(RMS)} = \frac{1-D}{(1+D)(1-3D)} I_{PN} \tag{32}$$

Therefore, the power loss in the inductor is given as

$$P_{rL\_loss} = I_{L1(RMS)}{}^2 r_{L1} + I_{L2(RMS)}{}^2 r_{L2} \tag{33}$$

Where r_{L1} and $r_{L2}$are the internal resistance of inductors.

2.11.2. Capacitor Power Loss

The capacitor power loss in EBASC-ZSI topology is obtained by multiplying its RMS currents with the capacitor internal resistance (r_C). The calculation of capacitor power loss is given below.

The currents in capacitor in ST state and NST state can be given as,

$$i_{C1} = \begin{Bmatrix} \frac{-(1-D)}{(1+D)(1-3D)} I_{PN}(0, DT_s) \\ \frac{D}{1-3D} I_{PN}(DT_s, T_s) \end{Bmatrix} \tag{34}$$

$$i_{C2} = \begin{Bmatrix} \frac{-(1-D)}{1-3D} I_{PN}(0, DT_s) \\ \frac{D(1+3D)}{(1+D)(1-3D)} I_{PN}(DT_s, T_s) \end{Bmatrix} \tag{35}$$

$$i_{C3} = \begin{Bmatrix} \frac{-(1-D)}{1-3D} I_{PN}(0, DT_s) \\ \frac{D}{1-3D} I_{PN}(DT_s, T_s) \end{Bmatrix} \tag{36}$$

Based on Equation (34), (35) and (36) the value of RMS capacitor current is given below,

$$I_{C1(RMS)} = \frac{\sqrt{D((1-D)(1+D^2) + D^2(1-D^2))}}{(1+D)(1-3D)} I_{PN} \tag{37}$$

$$I_{C2(RMS)} = \frac{\sqrt{D((1+D)(1+3D^2) - 8D^4)}}{(1+D)(1-3D)} I_{PN} \tag{38}$$

$$I_{C3(RMS)} = \frac{\sqrt{D(1-D)}}{1-3D} I_{PN} \tag{39}$$

Therefore, the total loss across capacitor is given as

$$P_{rC\_loss} = I_{C1(RMS)}{}^2 r_{C1} + I_{C2(RMS)}{}^2 r_{C2} + I_{C3(RMS)}{}^2 r_{C3} \tag{40}$$

Where r_{C1}, r_{C2} and r_{C3} are the internal resistance of three capacitors

2.11.3. Diode Power Loss

In the EBASC-ZSI topology the power loss in the diodes is consists up of reverse recovery loss (P_{rrD}) and conduction power loss .TheP_{rrD} due to three diodes in the EBASC-ZSI topology is given as, $P_{rrD} = 3.Q_{rr}.\hat{V}_{PN}.f_s$. Where f_s is the switching frequency and Q_{rr} is the diode reverse recovery charge. The average and RMS diode current is given as,

$$I_{D1(AVG)} = \frac{(1-D)^2}{1-3D} I_{PN}, I_{D1(RMS)} = \frac{(1-D)\sqrt{1-D}}{1-3D} I_{PN} \tag{41}$$

$$I_{D2(AVG)} = \frac{D(1-D)}{1-3D} I_{PN}, I_{D2(RMS)} = \frac{D\sqrt{1-D}}{1-3D} I_{PN} \tag{42}$$

$$I_{D3(AVG)} = \frac{(1+D^2)(1-D)}{(1+D)(1-3D)} I_{PN}, I_{D3(RMS)} = \frac{(1+D^2)\sqrt{1-D}}{(1+D)(1-3D)} I_{PN} \tag{43}$$

The forward voltage drop power loss is given as,

$$P_{V_F\_loss} = I_{D1(AVG)} V_F + I_{D2(AVG)} V_F + I_{D3(AVG)} V_F \tag{44}$$

The power loss due to r_{D1}, $r_{D2}$and $r_{D3}$is given as,

$$P_{r_D\_loss} = I_{D1(RMS)}{}^2 r_{D1} + I_{D2(RMS)}{}^2 r_{D2} + I_{D3(RMS)}{}^2 r_{D3} \tag{45}$$

Where r_{D1}, $r_{D2}$and r_{D3} are the internal resistance of diodes

Therefore, the total power loss associated with diode is,

$$P_{D\_loss} = P_{rrD} + P_{V_F\_loss} + P_{r_D\_loss} \tag{46}$$

2.11.4. Extra Switch Power Loss

The extra switch power loss occurred due to the use of an extra switch in the Z-impedance network of EBASC-ZSI. The extra switch losses used in the Z-impedance is divided into two parts i.e. the switching loss (P_{SW5}) and the conduction loss (P_{cond5}). The current through switch S_5 in ST state and NST state is given as,

$$i_{S_5} = \begin{Bmatrix} \frac{1-D}{1-3D} I_{PN}(0, DT_S) \\ 0, (DT_S, T_S) \end{Bmatrix} \tag{47}$$

The average and RMS current is given by,

$$I_{S_5(AVG)} = \frac{D(1-D)}{1-3D} I_{PN} \tag{48}$$

$$I_{S_5(RMS)} = \frac{(1-D)\sqrt{D}}{1-3D} I_{PN} \tag{49}$$

Therefore, the loss in switch S_5 is given as,

$$P_{SW5} = \frac{t_{on} + t_{off}}{2} f_{S_5} V_{S_5} i_{S_5} \tag{50}$$

$$P_{cond5} = I_{S_5(RMS)}{}^2 r_{S_5} \tag{51}$$

Where t_{on} and $t_{off}$are turn on and turn-off delay time of switch S_5, r_{S_5} is the resistance of switch S_5.

The numerical value of the above losses with considering the value of parasitic elements given in Table 3.

Table 3. Parasitic value of different parameter used for calculation of different losses in the Z-impedance

Parameter	Value
Inductors parasitic resistance (L1, L2)	0.12 Ω
ESR of capacitors(C1, C2, C3)	0.1 Ω
Diodes(RURG3060CC)	600V, 30 A, $V_{F(Max)}$=1.3 V
MOSFET S5(IXFH170N25X3)	250V, 170 A, $r_{S5(max)}$=7.4 Ω

Hence with the help from above parameter and input voltage, the numerical value of different losses with D=.1 is

Inductor loss = .14 W

Capacitor loss = .041 W

Diode loss = .84 W

Extra switch power loss = .032 W

Hence comparing the numerical value of the above losses it is found that the highest losses occurred is due to diode.

2.12. Economic Analysis of EBASC-ZSI

In converter topologies greater performance improvement could support a greater equipment cost. To increase the performance improvement, the system loss has to decrease. The system loss can be reduced with the increase in voltage and reduce in current so that the I^2R loss can be reduced.

The proposed EBASC-ZSI topology is a single stage converter unlike the dc-dc boost converter which operates on a two stage conversion system. The switching loss in a two stage converter is high due to its high frequency switching as compared to single stage converter. In two stage PV distributed generation (PVDG) system two separate converter are required for power extraction, grid synchronization and power flow control. However in single stage PVDG system, a single converter does the work of power extraction, grid synchronization and power flow control. Moreover in a two stage PVDG system two controllers are required to control two stages of the system i.e. voltage boosting and power conversion. However in case of single stage PVDG system one controller does the work of both voltage boosting and power conversion. Hence in a single stage PVDG system, complexity and losses can be reduced compared to two stages PVDG system. The performance efficiency comparison of EBASC-ZSI topology with respect to DC-DC boost converter has given below in Fig. 8.

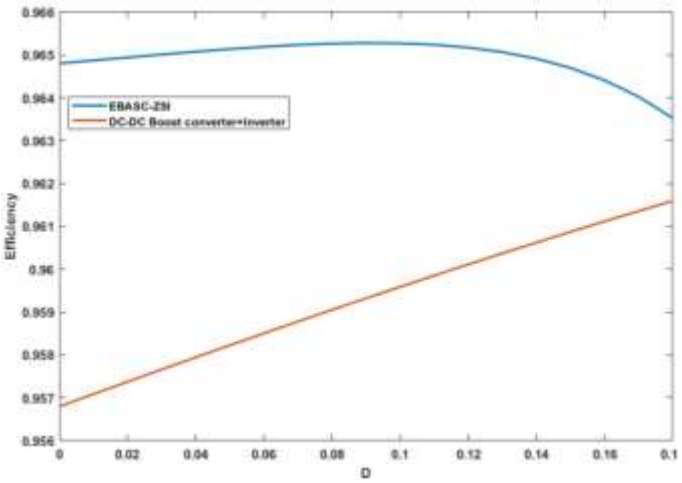


Fig. 8. Comparison of *D verses efficiency of* EBASC-ZSI topology and DC-DC boost converter at D=.1.

5. Simulation Results

The simulation of EBASC-ZSI topology is carried out using MATLAB/Simulink software. The parameters used for the simulation is shown in Table 4. The simulation results of EBASC-ZSI such as input voltage (Vdc), peak dc-link voltage (VPN), output voltage (Vo), voltage across C1 capacitor (VC1), voltage across C2 capacitor (VC2) are shown in Fig. 9. In Fig. 10 the waveforms of voltage across C3 capacitor (VC3), inductor L1 current (IL1), inductor L2 current (IL2) and switch S5 (SW5) waveforms are shown. It is to be noted that the results in Fig. 9 and Fig.10 have taken with the same ST state duty cycle (D) =.1 and same modulation index (M) =.9. In Fig. 11 the results of waveform Vdc, VPN, Vo, VC1and VC2 have taken. In Fig. 12 the results of waveform VC3, IL1, IL2 and SW5 have taken. It is to be noted that the results in Figure 11 and Fig. 12 have taken with D=.2 and M=.8. The simulation results obtained in Fig. 9 with Vdc of 25V and D=.1 is VPN = 35 V, Vo = 35 V, VC1 = 31 V and VC2 = 4 V. The simulation results obtained in Fig. 10 with Vdc of 25V and D=.1 isVC3= 31 V, IL1 =0.7 A, IL2= 0.55 A and pulse across SW5. The simulation results obtained in Fig. 11 with Vdc of 25V and D=.2 is VPN = 56 V, Vo = 56 V, VC1 = 45 V and VC2 = 11 V. The simulation results obtained in Figure 12 with Vdc of 25V and D=.2 is VC3= 45 V, IL1 = 1.8 A, IL2= 1.6 A and pulse across SW5. From the above results it is confirmed that the mathematical expression derived for different parameter of EBASC-ZSI topology is matching with the simulation results of the topology. Hence, it proves the worth of of topology.

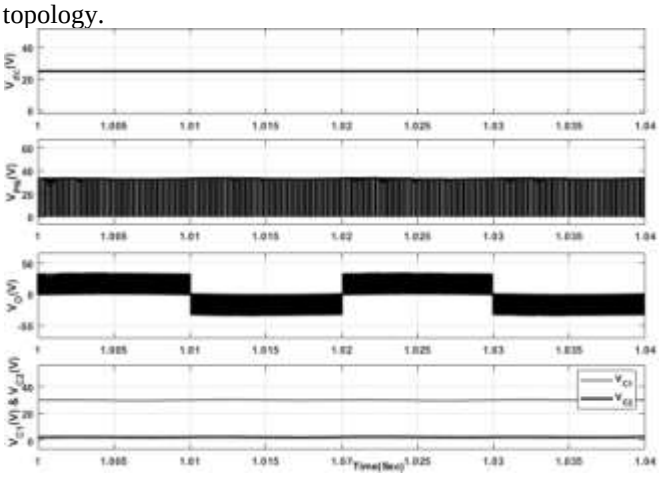


Fig. 9. Waveform of V_{dc},V_{PN}, V_o, V_{C1} and V_{C2} of EBASC-ZSI topology with D=.1.

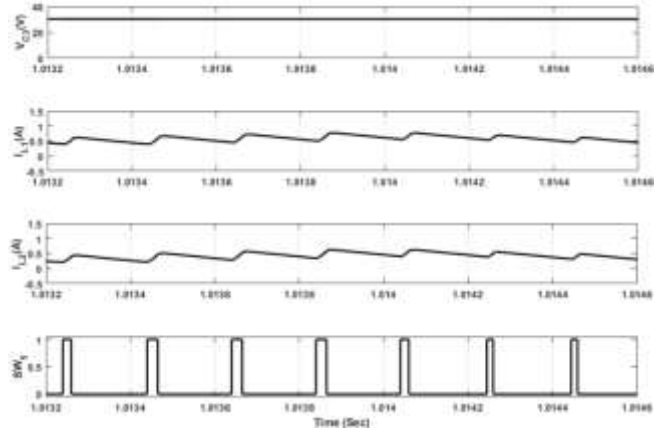


Fig. 10. Waveform ofV_{C3}, I_{L1}, I_{L2} and SW_5 of EBASC-ZSI topology with D=.1.

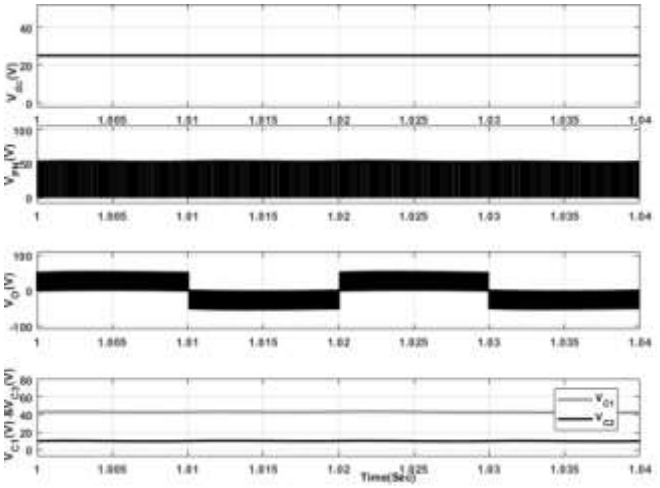


Fig.11. Waveform of V_{dc}, V_{PN}, V_o, V_{C1} and V_{C2} of EBASC-ZSI topology with D=.2.

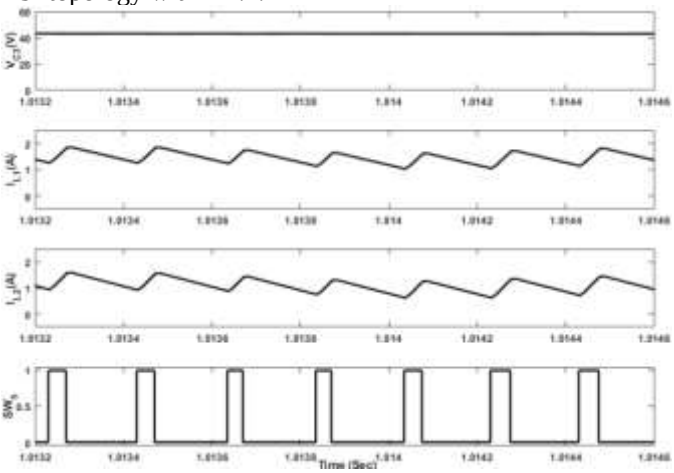


Fig. 12. Waveform ofV_{C3}, I_{L1}, I_{L2} and SW_5 of EBASC-ZSI topology with D=.2.

3. Experimental Results

The hardware prototype of EBASC-ZSI topology shown in Fig. 13 has been developed in the laboratory. The prototype has developed with the help of dc-voltage source, active and passive components like inductors, capacitors, diodes, inverter and a rheostat etc. For measurement of voltage and current in the circuit, AD2020JY amplifier and LEM current sensors is used. To provide switching pulse to the switches of the inverter, TMS320F28377S DSP controller is used. To record the waveform of EBASC-ZSI topology, a digital storage oscilloscope DSOX1204G is used. The parameters used for hardware prototype is shown in Table 4.

The experimental results of V_{dc}, V_o is shown in Fig. 14. In Fig. 14 (a) the experimental results of V_{dc} and V_o is taken at V_{dc} = 25V and D=.1 while in Fig. 14 (b) the experimental results of V_{dc} and V_o are taken with V_{dc} = 25 V, D =.2. The results in Fig. 14 (a) shows that by providing the input voltage of 25 V, the output voltage from the EBASC-ZSI topology is 32 V. The results in Fig. 14(b) shows that by providing the input voltage of 25 V, the output voltage from the EBASC-ZSI topology is 53V. The experimental results of I_{L1}, I_{L2}, V_{C1} and SW_5 is shown in Fig. 15. In Fig. 15 (a) the experimental results of I_{L1}, I_{L2}, V_{C1} and SW_5 is taken at V_{dc} = 25V and D=.1 while in Fig. 15 (b) the experimental results of I_{L1}, I_{L2}, V_{C1} and SW_5 are taken with V_{dc} = 25 V, D =.2. The results obtained in Fig. 15(a) are I_{L1} =.6 A, I_{L2} = .5 A, V_{C1} = 29 V and SW_5= 12 V. The results obtained in Fig. 15(b) are I_{L1} = 1.64 A, I_{L2} = 1.5 A, V_{C1} = 43 V and SW_5 = 12 V.

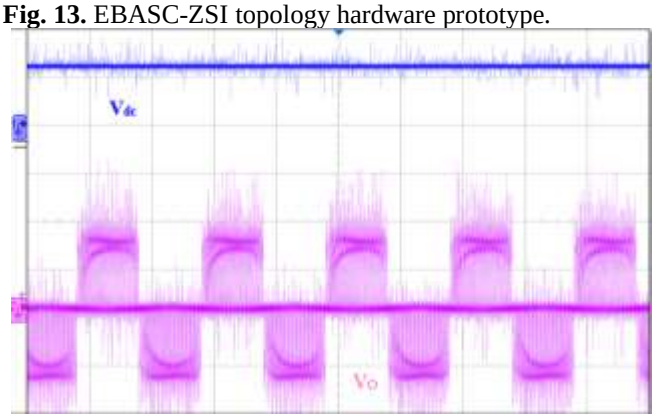
From the obtained experimental results, simulation results and the mathematical formulae of the EBASC-ZSI topology, it is clear that the three are matching with each other. Hence the topology proved its worthiness for future applications in a single stage PVDG system.

Table 4. The parameters and its value used in both hardware prototype and simulation of EBASC-ZSI topology.

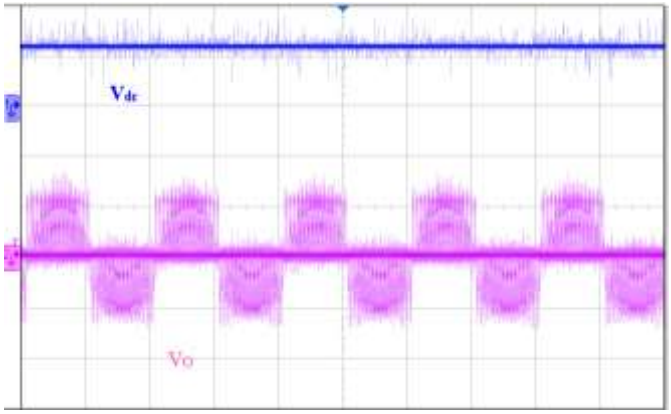
Parameter	Value
V_{dc}	25 V
f_o	50 Hz
f_s	5 kHz
L_1=L_2	3 mH
C_1=C_3, C_2	470 µF, 220 µF
R_l	50 Ω

Where V_{dc} is input voltage, f_o is fundamental frequency, f_s is switching frequency, L_1=L_2 is inductors, C_1=C_3, C_2 is Capacitors, R_l is load Resistance

Fig. 13. EBASC-ZSI topology hardware prototype.

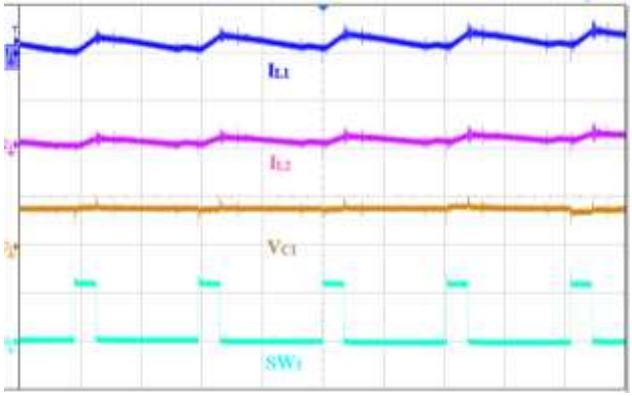


(a)

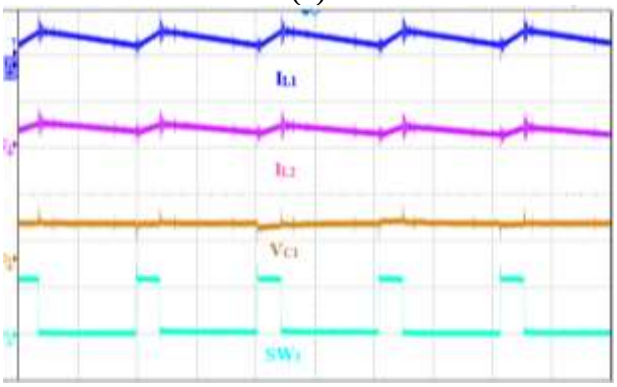


(b)

Fig. 14. Experimental results of V_{dc} and V_o of EBASC-ZSI topology (a) at D= .1, V_{dc} (20 V/div), V_o (20 V/div) (b) D=.2, V_{dc} (20 V/div), V_o (50 V/div).



(a)



(b)

Fig. 15. Experimental results of I_{L1}, I_{L2}, V_{C1}, and SW_5 (a) D= .1, I_{L1} (1 A/div), I_{L2} (1 A/div), V_{C1} (40 V/div), SW_5(10 V/div) (b) D= .2, I_{L1} (2 A/div), I_{L2}(2 A/div), V_{C1} (50 V/div), SW_5(10 V/div).

4. Conclusion

A new EBASC-ZSI topology is introduced and analysed in this paper. The topology provides higher voltage gain with lower value of shoot through state duty cycle. The topology is compared with several topologies in the field of ZSI. The topology mathematical modelling, Simulink modelling and hardware prototype is developed and presented in this manuscript. The matching of mathematical modelling, Simulink modelling and hardware prototype shows the effectiveness of the EBASC-ZSI topology. The EBASC-ZSI has similar or less current stress with some of the compared topologies but its voltage stress across some of the capacitor is similar or more with the compared topology.

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