Modelling and Real-time Validation of a Two–input High–gain DC–DC Converter with a Reduced Number of Switches

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Abstract- Power electronic converters play a major role in different applications such as power generation, transmission, distribution, and emerging electric vehicle (EV) technology. Among different types of power electronic converters, DC-DC converters are taking a crucial responsibility in renewable energy resources-based power generation (RERPG) and EV applications, as there is a huge variation between output and input voltage levels. In this article, the operation and modelling of a dual-input high-gain DC–DC converter with a reduced number of switching elements are discussed. The diode–capacitor voltage multiplier (DCVM) cells are utilized in the suggested converter to achieve the ultra-high gain. Because of the lower number of power semiconductor switches and better design, the designed converter exhibits 97.09% efficiency at the selected duty cycle and power rating. To validate the design, a hardware setup is also produced and tested effectively with OPAL-RT OP5700 real-time simulator (Hardware-in-the-loop). By using this converter, RERPG, and EV systems gain the advantage of lower number of switches, high gain, simple design, minimal voltage stress, and higher efficiency.

Keywords DC-DC power converter, power electronics switches, modelling, gain, real-time validation.

1. Introduction

Power conversion circuitry is needed to accept the power from various sources, convert it as per the load requirement and send that energy to the load, as the utilization of sources of clean energy grows. The development of energy conversion systems has been made more difficult by the necessity to receive power from various resources, such as fuel cells, photovoltaic (PV) cells and wind energy conversion systems, all of which operate at varying voltages and current levels, and convert that energy to a controlled voltage [1–6]. Multi-input DC-DC converters (MIC) are created to address this issue. As shown in Figure 1, an incorporated multi-input converter is able to be utilized in place of numerous DC–DC converters that are connected to various sources individually. These converters are designed with low component counts, lowered volume and expense, and improved dynamic functionality [7]. Due to the presence of storage units in certain applications, multi-input converters are required to provide an electricity flow route through additional sources or a direct current (DC) link to supply electricity for the charging of the storage devices [7–14].

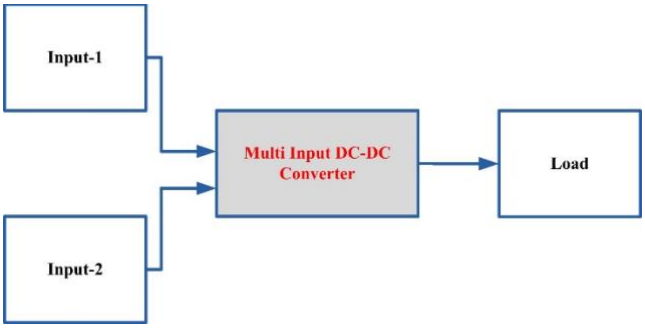

Fig. 1. Basic block diagram of multi-input DC-DC converter incorporated system.

Multi-input converters can be isolated or non-isolated depending on the purpose [15]. Non-isolated DC–DC converters are preferable in situations where isolation may not be necessary, such as in low-power hybrid-electric

automobiles or solar energy systems. High step-up methodologies are required to be employed in applications involving hybrid vehicles and clean energy sources where the input voltage is minimal [16–18]. Non-isolated multi-input DC–DC converters have recently been introduced in articles.

The authors of [19] published a novel MIC topology with the battery as one of the inputs. Regrettably, the power electronic switches are going through considerably higher voltage stress. A new MIC topology is established in [20] for EV applications. In this topology, multiple relays are utilized to achieve the required operation. This increases the complexity of the circuit. In [21], the researchers developed an ultra-high gain MIC for photovoltaic (PV) panels-powered EVs, but the component count and losses are high. Concurrently, this converter is not capable of delivering power to the battery and load. In [22], the researchers published a new bridge-type MIC for incorporating non-conventional resources. It can produce higher gain with the help of both bidirectional and unidirectional switches but the switching stress is high. It also exhibits the opposite polarity at the output terminals. The researchers of [23] depict a MIC with bidirectional power flow capability. But the count of switches is higher, and the battery should be one of the inputs. The article [24] illustrates the design and validation of a MIC with a lower component count and it also exhibits the lower voltage stress across the switches. Unfortunately, the losses in the converter are high, along with the component count. The authors illustrated a novel high-gain modular MIC in [25]. On the other hand, the component count and voltage stress are really high. Moreover, this converter's number of memory elements is high, so the control circuit design is very complex. In [26], the researchers developed a MIC for low and medium-power renewable energy systems. This non-isolated converter has greater gain at fewer circuit components, but the voltage stress is still high. Furthermore, the count of memory elements remains high, which makes the control design complex. Even though there are multiple types of MICs in the previous studies, there is a crucial need for developing a novel MIC with higher gain, higher efficiency, lower stress, and lower component count for renewable energy resources and EV applications.

In this article, chapter 2 illustrates the working modes of the designed converter. In Chapter 3, the steady-state modelling and stability analysis of the designed converter. The OPAL-RT-based experimental findings are discussed in Chapter 4. Finally, the last nail of the proposed work is hammered in Chapter 5.

2. Proposed Converter

The configuration of the proposed two-input high-gain DC–DC converter is shown in Figure 2. In the proposed topology, S_1 & S_2 are the semiconductor switches and V_1 & V_2 are the input voltages. I_{L1} & I_{L2} and V_{L1} & V_{L2} are the currents and voltages of inductors L_1 & L_2, respectively. Similarly, I_{C1}, I_{C2} & I_{C0} and V_{C1}, V_{C2} & V_0 are the currents and voltage of capacitors C_1, C_2 & C_0, respectively. R is the load resistance, and V_0 is the output voltage. The diodes D_1, D_2 & D_3 are utilized in the suggested converter.

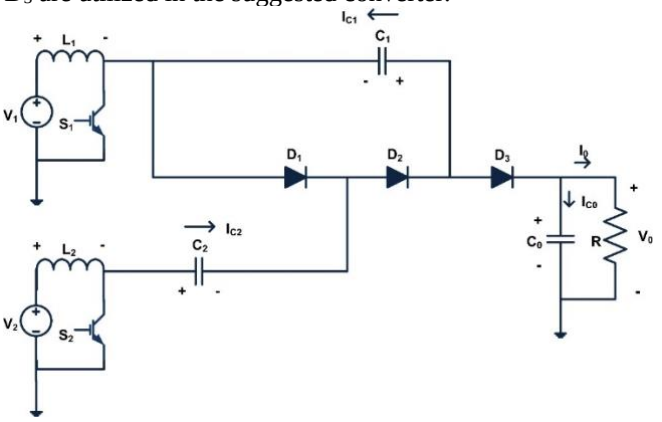

Fig. 2. Proposed two-input high-gain DC–DC converter with a reduced number of switches.

Three DCVM cells are employed in the designed topology to stretch the output voltage. This high output voltage can successfully apply to RERPG and EV applications. The operation of the suggested converter is discussed below.

The designed converter technically has three operating modes. As per the mentioned applications, assume the proposed converter operates under continuous conduction mode (CCM). T and f are the time period and frequency of the switching sequence, respectively. The time intervals of respective operating modes are δ_{1T}, δ_{2T}, and $(1-\delta_{1T}-\delta_{2T})$. d_1 and d_2 are the duty ratios of switching pulses of S_1 and S_2, respectively.

2.1. Mode-1 ($0<t<\delta 1T$)

Figure 3(b) displays the Mode-2 operation of the designed topology. In this mode of operation, S_1 continues its ON state, and the state of S_2 changes to OFF. L_1 continue its charging state, and C_1 starts charging through D_2 with the help of energy from V_2, L_2 & C_2. Still, the C_0 is discharging through R.

2.2. Mode-2 ($\delta 1T < t < (\delta 1T+\delta 2T)$)

Figure 3(b) displays the Mode-2 operation of the designed topology. In this mode of operation, S_1 continues its ON state, and the state of S_2 changes to OFF. L_1 continue its charging state, and C_1 starts charging through D_2 with the help of energy from V_2, L_2 & C_2. Still, the C_0 is discharging through R.

2.3. Mode-3($(\delta 1T+\delta 2T)<t< T$)

Figure 3(c) shows the Mode-3 operation of the designed topology. In this mode of operation, the state of S_1 changes to OFF, and the state of S_2 changes to ON. L_2 is in charging condition, and C_2 charges through D_1 with the help of V_1 and L_1. V_1, L_1 & C_1 together supply power to load R.

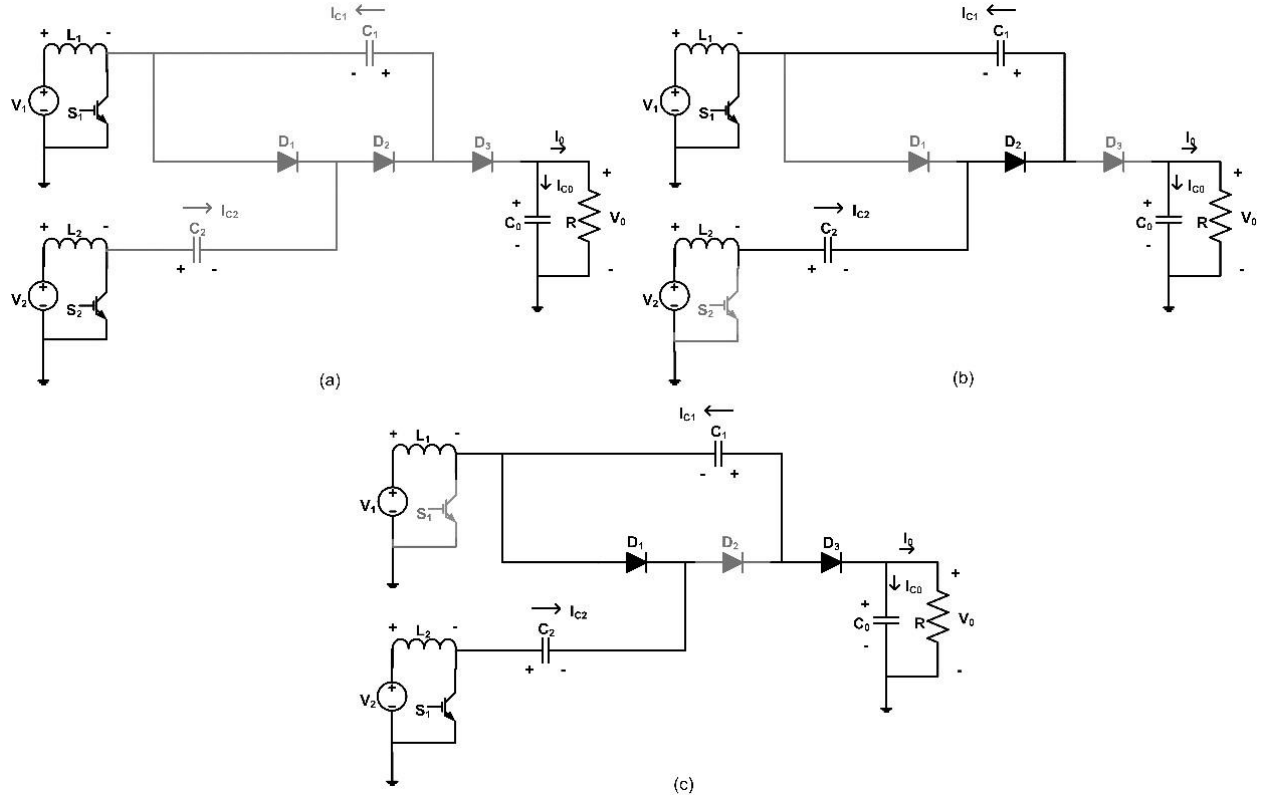

Fig. 3. Modes of operation: (a) Mode-1, (b) Mode-2, (c) Mode-3.

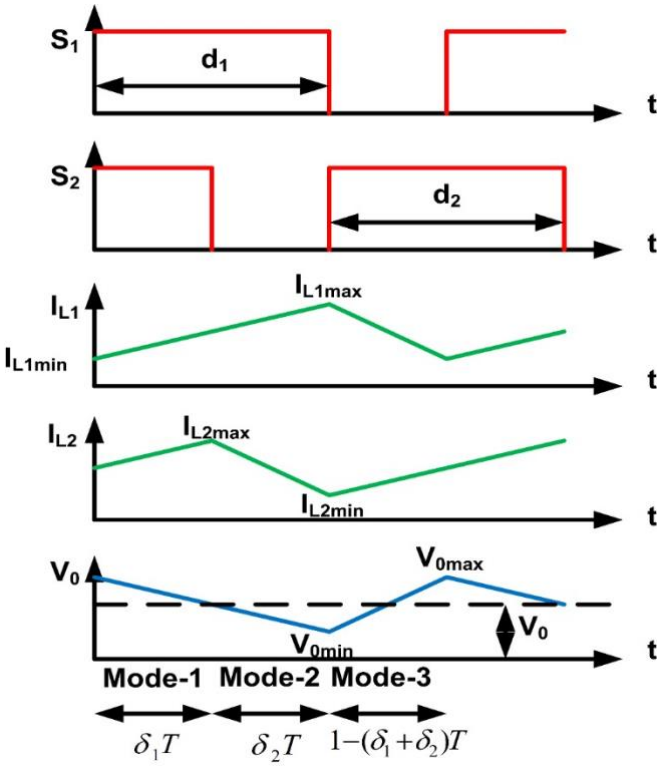

Fig. 4. Ideal waveforms of the proposed converter under CCM.

Figure 4 shows the I_{L1}, I_{L2}, and V_0 waveforms of the designed converter in ideal conditions with respect to duty ratios d_1 and d_2. The mathematical background of the proposed converter, along with the memory elements selection, is discussed in the following section.

3. Steady State Modelling

The continuous conduction mode (CCM) of the proposed converter is discussed in this research article. Steady-state modelling illustrates the mathematical modelling of the proposed converter topology under steady-state conditions. Here, I_{L1min} & I_{L1max}, I_{L2min} & I_{L2max} and V_{0min} & V_{0max} are the minimum and maximum values of I_{L1}, I_{L2}, and V_0 respectively.

Under Mode-1, the mathematical expression of the inductor voltages is displayed in equations (1) & (2).

$$V_{L1} = V_1 \tag{1}$$

$$V_{L2} = V_2 \tag{2}$$

The mathematical equations of the current flowing through load resistor R are displayed in (3) and (4).

$$I_0 = V_0/R \tag{3}$$

$$I_0 = -I_{C0} = V_0/R \tag{4}$$

The slope expressions of inductor currents, capacitor voltages and output voltage are shown in equations (5), (6), (7), (8) & (9).

$$dI_{L1}/dt = V_1/L_1 \tag{5}$$

$$dI_{L2}/dt = V_2/L_2 \tag{6}$$

$$dV_{C1}/dt = 0 \tag{7}$$

$$dV_{C2}/dt = 0 \tag{8}$$

$$dV_0/dt = (-V_0)/RC_0 \tag{9}$$

Under Mode-2, the mathematical expression of the inductor voltages are displayed in equations (10) & (11).

$$V_{L1} = V_1 \quad (10)$$

$$V_{L2} = V_2 - V_{C1} - V_{C2} \quad (11)$$

The mathematical equations of the current flowing through load resistor R are displayed in equations (12) and (13).

$$I_0 = V_0/R \quad (12)$$

$$I_0 = -I_{C0} = V_0/R \quad (13)$$

The slope expressions of inductor currents, capacitor voltages and output voltage are shown in equations (14), (15), (16), (17) & (18).

$$dI_{L1}/dt = V_1/L_1 \quad (14)$$

$$dI_{L2}/dt = (V_2 - V_{C1} - V_{C2})/L_2 \quad (15)$$

$$dV_{C1}/dt = I_{L1}/C_1 \quad (16)$$

$$dV_{C2}/dt = I_{L1}/C_2 \quad (17)$$

$$dV_0/dt = (-V_0)/RC_0 \quad (18)$$

Under Mode-3, the mathematical expression of the inductor voltages are displayed in equations (19) & (20).

$$V_{L1} = V_1 + V_{C2} \quad (19)$$

$$V_{L2} = V_2 \quad (20)$$

The mathematical equations of the current flowing through load resistor R are displayed in equations (21) and (22).

$$I_0 = V_0/R \quad (21)$$

$$I_0 = -I_{C1} - I_{C0} = V_0/R \quad (22)$$

The slope expressions of inductor currents, capacitor voltages and output voltage are shown in (23), (24), (25), (26) & (27).

$$dI_{L1}/dt = (V_1 + V_{C2})/L_1 \quad (23)$$

$$dI_{L2}/dt = V_2/L_2 \quad (24)$$

$$dV_{C1}/dt = (I_{L1} - (V_0/R))/C_1 \quad (25)$$

$$dV_{C2}/dt = V_0/RC_2 \quad (26)$$

$$dV0/dt = (I_{L1}/C_1) - (2V_0/RC_2) \quad (27)$$

The resultant of Volt - Sec balance equation at L_1 is given by (28)

$$V_1 + (V_{C2} * (1 - \delta_1 - \delta_2)) = 0 \quad (28)$$

The resultant of Volt - Sec balance equation at L_2 is given by (29)

$$V_2 = (V_0 * \delta_2) + (2 * V_{C2} * \delta_2) \quad (29)$$

By simplifying the equations (28) and (29), the mathematical expression for V_0 can be derived as shown in equations (30) and (31).

$$V_0 = (V_2/\delta_2) + (2 * V_1/(1 - \delta_1 - \delta_2)) \quad (30)$$

The V0 expression in terms of duty ratios d_1 and d_2 is given by (31).

$$V_0 = V_2/(1 - d_1)) + (2 * V_1/(1 - d_2) \quad (31)$$

3.1 Stability

The stability of the proposed converter can be determined by the characteristic equation. To find the characteristic equation, system matrix A is required. To find the system matrix A, the state-space representation of the proposed system is formulated as shown in equations

$$\begin{bmatrix} \frac{dI_{L1}}{dt} \\ \frac{dI_{L2}}{dt} \\ \frac{dV_{C1}}{dt} \\ \frac{dV_{C2}}{dt} \\ \frac{dV_0}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{(1-\delta_1-\delta_2)}{L_1} & 0 \\ 0 & 0 & \frac{-\delta_2}{L_2} & \frac{-\delta_2}{L_2} & 0 \\ \frac{(1-\delta_1-\delta_2)}{C_1} & \frac{\delta_2}{C_1} & 0 & 0 & \frac{-(1-\delta_1-\delta_2)}{RC_1} \\ 0 & \frac{\delta_2}{C_2} & 0 & 0 & \frac{(1-\delta_1-\delta_2)}{RC_2} \\ \frac{(1-\delta_1-\delta_2)}{C_1} & 0 & 0 & 0 & -\frac{\delta_1+\delta_2}{RC_0} - \frac{2(1-\delta_1-\delta_2)}{RC_2} \end{bmatrix} \times \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (32)$$

$$[V_0] = [0 \quad 0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_0 \end{bmatrix} \quad (33)$$

To simplify the calculations, consider C_1=C_2=C_0=C. The characteristic equation of the suggested converter is,

$$|A - SI| = 0$$

$$L_1L_2C^3RS^5 + L_1L_2C^2(2 - \delta_1 - \delta_2)S^4 + 2L_1C^2R{\delta_2}^2S^3 +$$

$$\left(2L_1C{\delta_2}^2(2 - \delta_1 - \delta_2) - L_2C(1 - \delta_1 - \delta_2)^3\right)S^2 +$$

$$RC{\delta_2}^2(1 - \delta_1 - \delta_2)^2S + {\delta_2}^2(\delta_1 + \delta_2)(1 - \delta_1 - \delta_2)^2 = 0 \quad (34)$$

The general form of characteristic equation of the fifth order system is given in equation (35).

$$aS^5 + bS^4 + cS^3 + dS^2 + fS + e = 0 \quad (35)$$

Where, S is the laplace transform variable.

As described below, the R-H Stability Criterion (RHSC) concept is utilized to understand the stability of the suggested converter topology. By comparing the equations (34) and (35), perform the R-H Stability Criterion (RHSC) concept to find the stability of the designed topology.

$$\begin{array}{c|cc} S^5 & a & c & f \\ & b & d & e \\ S^4 & \frac{bc-ad}{b} & \frac{bf-ae}{b} & 0 \\ S^3 & \frac{bcd+abe-ad^2-fb^2}{bc-ad} & e & 0 \\ S^2 & \frac{(bcd+abe-ad^2-fb^2)(bf-ae)-e(bc-ad)^2}{b(bcd+abe-ad^2-fb^2)} & 0 & 0 \\ S^1 & e & 0 & 0 \\ S^0 & & & \end{array}$$

According to the derived RHSC table and RHSC, the proposed converter is stable. The proposed converter exhibits this stability under any duty cycle value below its maximum value.

3.2 Memory elements selection

The inductors L_1 & L_2 design equations are formulated as per the conventional method of calculating inductor values in conventional DC-DC converters. The inductors L_1 & L_2 design formulas are given in the following equations.

$$L_1 = V_1 * (\delta_1 + \delta_2)/(f * \Delta I_{L1}) \quad (36)$$

$$L_2 = V_2 * \delta_1/(f * \Delta I_{L2}) \quad (37)$$

The design and selection of capacitors C_1, C_2 & C_0 are done with the help of equation (38)

$$C_1 = C_2 = C_0 = V_0 * (\delta_1 + \delta_2)/(f * R * \Delta V_0) \quad (38)$$

4. Results and Analysis

The steady-state response of the designed DC-DC converter topology in CCM is discussed in this chapter. The selected switching frequency of the proposed converter is 10kHz, so the Isolated-gate bipolar transistors (IGBTs) are utilized.

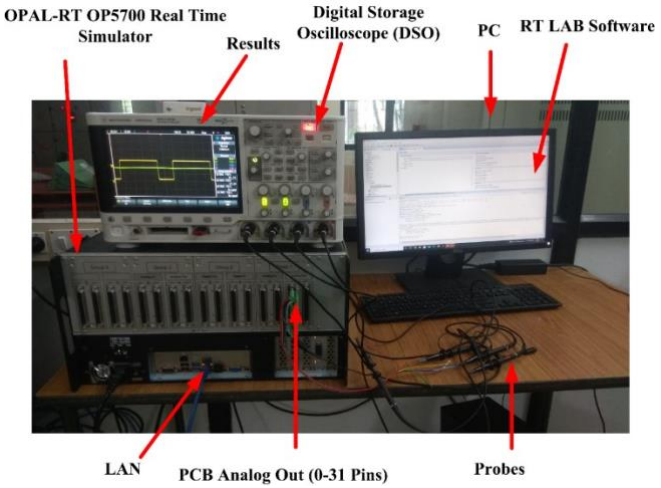

Fig. 5. An OPAL-RT OP5700 real-time simulator-based hardware setup of the proposed converter.

Table 1. OPAL-RT Simulator (Hardware-in-the-loop) specifications

Parameter/Component	Specifications
Device	OP5700
CPU	Intel® Xeon® E5, 4 core / 3GHz to 32 cores / 2.3GHz
Electrical ratings	Input: 100–240*VAC*, 50–60*Hz*, 10/5*A* Power: 600*W*
FPGA	Xilinx® Virtex®7 FPGA on VC707 board Processing speed: 200*ns*–2*μs*
I/O lines	256 lines
Channels	16 or 32
I/O connectors	4 panels of BD37 connectors
High-speed communication ports	16 SFP sockets, Up to 5 GBps
Monitoring connectors	4 panels of RJ45 connectors
PC interfaces	Standard PC connectors
Minimum possible sampling time	1μs
Software	RT-LAB

A laboratory-based hardware setup is implemented with the help of an OPAL-RT OP5700 real-time simulator to investigate the suggested converter's effectiveness. Initially, the mathematical modeling of the proposed converter is validated successfully in the MATLAB/Simulink environment under a fixed-step solver. The fixed-step mode validated MATLAB model of the proposed converter is uploaded in the RT-LAB software which is necessary for interfacing the MATLAB environment with the OPAL-RT environment. The employed OPAL-RT OP5700 real-time simulator's specifications are mentioned in Table 1. The minimum possible sampling time of this real-time simulator is 1μs. In order to get proper shapes of the required waveforms with minimum distortions as like theoretical waveforms as displayed in Figure 4, the designed converter topology is operated at a sampling time of 5μs. Depending on the selected sampling time, the switching frequencies is calculated as f_{sS}=10kHz. The first input voltage is considered as V_1=36V, and the second input voltage is V_2=48V. By using V_1 and V_2 the suggested converter is modelled to operate at 400V and 1000W. The real-time simulator-based hardware setup of the suggested topology is displayed in Figure 5. The design specifications of the suggested converter are given in Table 2.

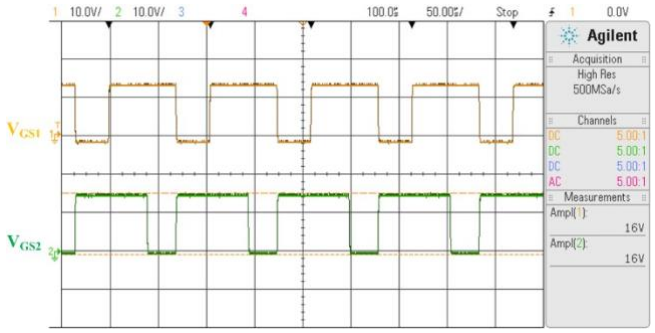

Fig. 6. Hardware investigation: waveforms of gate pulses of applied at S_1 and S_2.

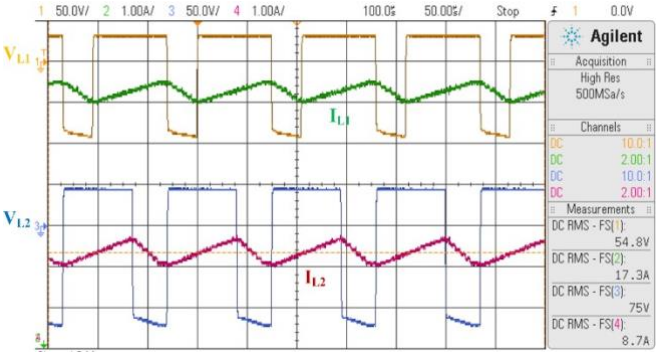

Fig. 7. Hardware investigation: Waveforms of inductor currents and voltages.

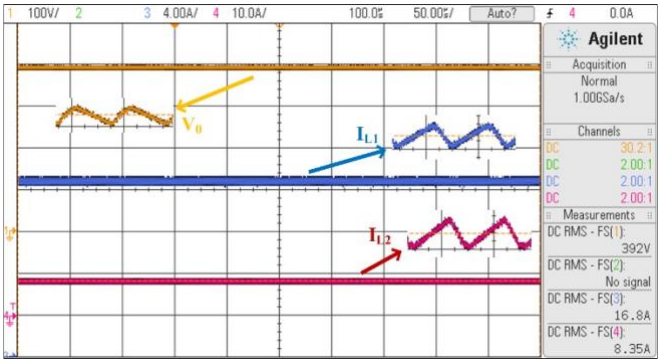

Fig. 8. Hardware investigation: waveforms of inductor currents and output voltage.

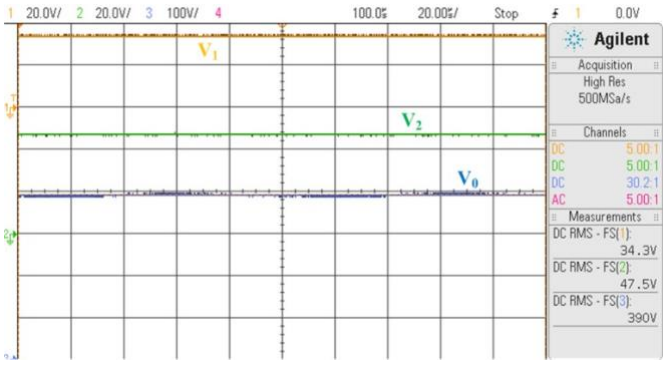

Fig. 9. Hardware investigation: waveforms of input and output voltages.

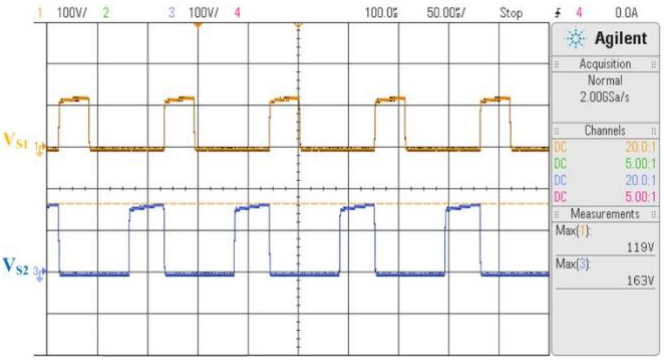

Fig. 10. Hardware investigation: waveforms of voltage stress of S_1 and S_2 switches.

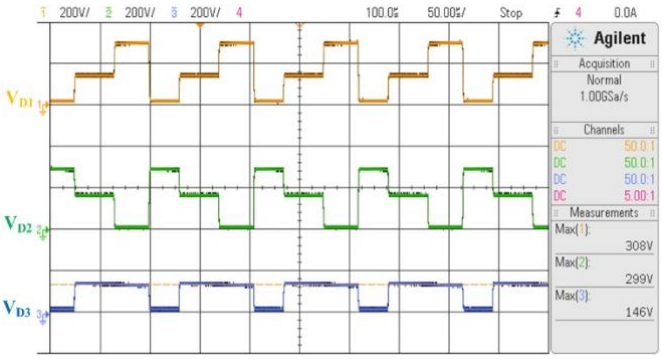

Fig. 11. Hardware investigation: waveforms of voltages across diodes D_1, D_1 and D_3.

Figure 6 shows the experimental pulses supplied at the gate of switches S_1 and S_2. From Figure 6, the amplitude of the pulses is V_{GS1}=V_{GS2}=16V with 10kHz switching frequency at 0.7 duty cycle. Figure 7 shows the resulted waveforms of inductor currents and voltages during the investigation of the real-time simulator-based hardware setup of the designed converter. From Figure 7, the DC RMS quantities of V_{L1}, V_{L1}, I_{L1} and I_{L2} are 54.8V, 75V, 17.3A and 8.7A. The experimental waveforms of inductors charging and discharging are nearly the same as theoretical waveforms as shown in the operation of the suggested converter.

Figure 8 displays the experimental results of inductor currents and output voltage of the proposed converter. From Figure 8, the DC RMS value of V_0 is 392V. Figure 9 displays the experimental waveforms of input voltages supplied to the proposed converter and respective output voltage at the designed duty cycle. From Figure 9, the DC RMS values of input voltages are V_1=34.3V, V_2=47.5V and the respective DC RMS value of output voltage V_0 is 392V. Figure 10 displays the voltage waveforms across S_1 & S_2 while performing the experimentation. These waveforms help to find the voltage stress (maximum voltage developed across the power electronics switch, when it is in OFF state) of the switch. The voltage stress values of the switches S_1 and S_2 are V_{S1}=119V and V_{S2}=163V respectively. Figure 11 shows the experimental waveforms of the voltage across the diodes D_1, D_2 and D_3. In the selected time period, V_{D1}, V_{D2} and V_{D3} are the maximum voltages (voltage stress) across the diodes D_1, D_2 and D_3 respectively. From Figure 11, V_{D1}=308V, V_{D2}=299V and

V_{D3}=146V. Figure 12 and Figure 13 represent the respective output voltage variation and efficiency variation with respect to the duty cycle. From Figure 12, the output voltage of the designed topology can reach up to 1182V at the maximum value of δ_1. From Figure 13, the maximum possible efficiency of the designed topology is 97.09% at 0.733 duty cycle and the efficiency will vary from 89.95% to 97.09%.

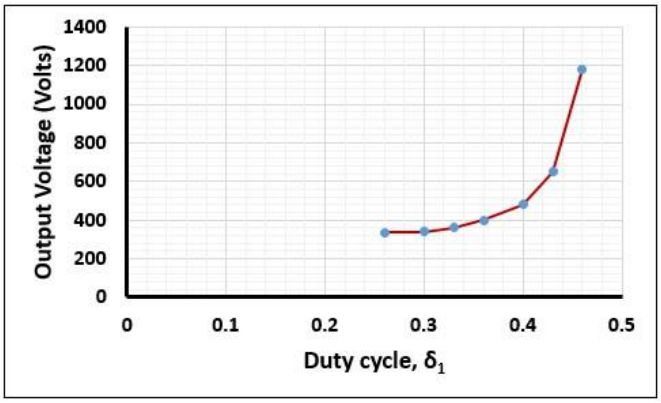

Fig. 12. Output voltage variation with respect to duty cycle.

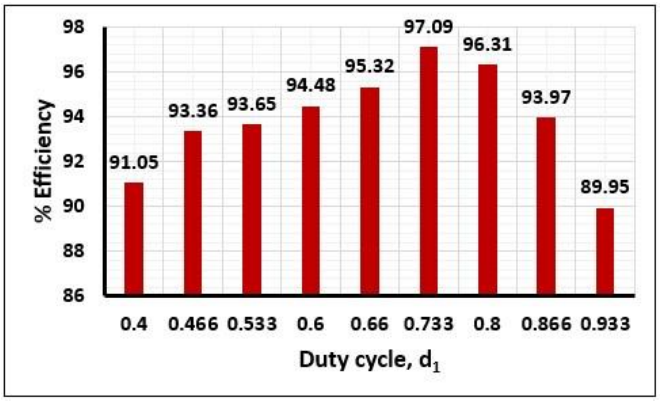

Fig. 13. Efficiency variation with respect to duty cycle.

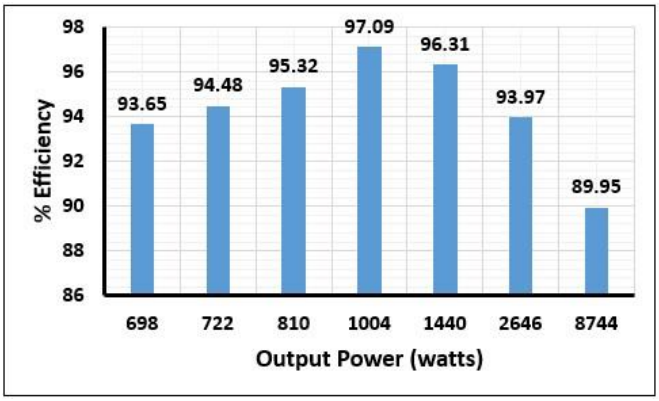

Fig. 14. Efficiency variation with respect to Output power.

The variation of the % Efficiency with respect to output power is displayed in Figure 14. The suggested topology exhibits 97.09% maximum efficiency at the designed power rating. From Table 3, compared to the existing converters, the designed topology is competent at the power semiconductor component's count, gain, voltage stress and efficiency.

In Table 3,

$$G_{11} = V_0 = \frac{(d_1 + d_2)V_1 + d_2V_2}{1 - d_1 - d_2}$$

$$G_{12} = V_0 = \frac{d_1V_1 + d_2(V_1 + V_2) + d_3V_2}{1 - d_1 - d_2 - d_3}$$

$$G_{13} = V_0 = \frac{d_1V_1 + (1 - d_1)V_2}{1 - d_2}$$

$$G_{14} = V_0 = -\frac{d_1V_1 + d_2V_2 + d_3(V_1 + V_2)}{1 - d_1 - d_2 - d_3}$$

During discharging

$$G_{15} = V_0 = \frac{d_1V_{battery} + (1 - d_1)V_1 + (1 - d_2)V_2}{1 - d_3}$$

During charging

$$G_{16} = V_0 = \frac{-d_1V_{battery} + V_1 + (1 - d_2)V_2}{1 - d_3}$$

$$G_{17} = V_0 = \frac{(2 - d_1)V_1 + V_2}{(1 - d_1)^2}$$

$$G_{18} = V_0 = \frac{d_1 + d_3 + d_5}{1 - d_1 - d_3 - d_5}\big(V_1(1 - d_3 - d_4) + V_2(1 - d_1 - d_2)\big)$$

$$G_{19} = V_0 = \frac{d_1 + d_2 + d_3}{1 - d_1 - d_2 - d_3}\big(V_1(d_1 + d_3) + V_2(d_2 + d_3)\big)$$

$$G_{20} = V_0 = V_2/(1 - d_1)) + (2 * V_1/(1 - d_2)$$

Table 3. Comparison with the state-of-the-art.

Converter	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	Proposed
Output voltage	G_{11}	G_{12}	G_{13}	G_{14}	G_{15}, G_{16}	G_{17}	G_{17}	G_{17}	G_{18}	G_{19}	G_{20}
No. of inputs	2	2	2	2	3	2	2	2	2	2	2
No. of power electronic switches	3	4	3	4	6	8	4	3	4	4	2
Count of diodes	5	3	1	0	2	2	4	3	1	2	3
Voltage stress	High	-	-	High	Low	High	Moderate	Moderate	Moderate	Moderate	Low
Total no. of memory elements	4	2	2	2	2	8	8	6	4	4	5
% Efficiency	93.5	94	93	94	88-94	91	95	94	95.5	96	97.09

5. Conclusion

In this article, the design and validation of a dual-input high step-up DC–DC converter with a reduced number of switching elements are discussed. In the designed converter, diode–capacitor voltage multiplier (VM) cells are utilized to achieve the ultra-high gain. Because of the less number of switches and better design, the designed converter exhibits 97.09% efficiency at the selected duty cycle and power rating. An OPAL-RT OP5700 real-time simulator (Hardware-in-the-loop) based hardware setup is developed to validate the design and operation of the proposed converter. The proposed converter gains the advantage of less number of switches, high gain, simple design, minimal voltage stress, and higher efficiency. The designed converter is better suitable for low and medium-powered RERPG and EV systems.

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