Control of T-Type Neutral Point Clamped Inverter for Solar Grid Connected System with Artificial Neural Network Controller

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Abstract: In grid-connected photovoltaic applications, three-phase multi-level inverters (MLI) such as Neutral point clamped (NPC), Flying capacitor (FC), and full bride inverters (FBI) are more popular in medium voltage drive applications. However, the main drawback is leakage current (LC) flowing through inverter leading to common mode voltage (CMV), current waveform distortion, and reduction in the system's overall performance. In this article transformer less grid connected NPC inverter (TLGC-NPCI) and transformer less T-type grid connected NPC inverter (T^3LGC-NPCI) is presented. T^3LGC-NPCI offers numerous advantages over TLGC-NPCI, including less LC and CMV, minimum requirement of gate drive signals leads to reduce switching and conduction losses. The multi-objectives of the suggested work are (i) maintaining constant DC-Link (DCL) voltage during different solar irradiation and constant temperature using artificial neural network controller (ANNC) (ii) Space vector pulse width modulation (SVPWM) technique is implemented to reduce LC flowing through inverter and to maintain constant CMV, and (iii) the reduction in total harmonic distortion (THD) of load current. The performance analysis of the proposed system was done in Matlab/ Simulink platform. A comparative analysis with the available methods like the Proportional integral Controller (PIC) was carried out to exhibit the viability of the developed control technique.

Keywords- Common mode voltage, Leakage Currents, Transformer less Inverter, Photovoltaic system, three-level NPC, Power Quality, THD.

Nomenclature

ANNC	Artificial Neural Network Controller
CMV	Common Mode Voltage
DCL	DC Link Voltage
EMI	Electro Magnetic Interference
FBI	Full Bridge Inverter
FC	Flying Capacitor
HERIC	Highly Efficient and Reliable Inverter Concept
IGBT	Insulated Gate Bipolar Thyristor
LC	Leakage Current
MLI	Multi-Level Inverter
MPPT	Maximum Power Point Tracking
NPCI	Neutral Point Clamped Inverter
NPV	Neutral Point Voltage
PIC	Proportional Integral Controller
PLL	Phase Locked Loop
PSO	Particle Swarm Optimization
PWM	Pulse Width Modulation
SRF	Synchronous Reference Frame
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
TLPV	Transformerless Photovoltaic
TLGC-NPCI	Transformerless Grid Connected - Neutral Point Clamped Inverter
T^3LGC-NPCI	Transformerless T-Type Grid Connected Neutral Point Clamp Inverter
C_{SPV}	Stray Capacitance of PV Array
a_f	Over loading factor in per unit
$I_{Leakage}$	Leakage Current
$I_{cr, pp}$	Ripple Current
m	Modulation Index
V_{dc}	The DC-Link Voltage
$V_{dc, Min}$	Minimum DC-Link Voltage

1. Introduction

Multi-level converter technologies have experienced significant advancements over the past few decades and have found widespread adoption in practical engineering applications. This popularity stems from their attributes, including high efficiency, lightweight design, ease of operation, compact size, and minimal conduction and switching losses.

1.1 Literature Review

For a three-phase grid-connected application, a novel transformer less topology H8 is designed by using logic functions [1] to control the entire modulation index and resulting in reduced stress on the output filter inductors and

low THD in the output grid current, minimizing the variation in CMV during inverter operation. Furthermore, the proposed topology can limit the LC according to the German standard DIN VDE 0126-1-1. By using this topology heat sink requirement is significant ac, and an additional number of devices achieves dc bypass.

PV inverters with isolation transformer were illustrated to discuss the challenges, which is bulky and difficult to install. To address these issues, TLPV inverters have gained popularity. These inverters are compact, cost-effective, and highly efficient since they eliminate the need for a bulky isolation transformer. However, one potential drawback of TL inverters is the lack of galvanic isolation between the PV panel and the grid. This absence of isolation can lead to the flow of common mode leakage current through the PV panel's parasitic capacitance.[2] Typical values of this parasitic capacitance range from 10 to 150nF for 1kW of power. Factors such as stray capacitance value and CM voltage variations play crucial roles in determining the magnitude of these LCs. To ensure the safety and proper operation of PV systems, the VDE 0126-1-1 mandates that if the LC exceeds 300 mA, the system must be disconnected from the grid. This disconnection helps to prevent electrical hazards, protect personnel, and avoid damage to the PV system and the grid. The reliability of grid-feeding or stand-alone inverter systems is a significant concern, and the impact of DCL capacitors on the system's overall reliability is explored. The study focuses on a three level DC-DC converter connected to a single-phase NPC inverter [3]. Two different Pulse Width Modulation (PWM) switching schemes are studied to minimize current ripple stress on the DCL capacitor to enhance the reliability. Various new inverter topologies have been proposed to eliminate the use of a grid isolation transformer to enhance the reliability efficiency, practicality and of PV systems. The NPC topology [4] advantage in transformer-less PV applications is low LC, high efficiency and reduced electromagnetic interference (EMI). In TLPV systems, the reduction of LC is a significant concern. Various single-phase H5, H6 and HERIC dc-bypass TLPV inverters have been proposed to address this issue, and it is widely accepted that the clamping topology is more effective than the unclamping topology in reducing LC and the reduction capabilities of three-phase TL inverter with clamping and unclamping dc-bypass switch [5].

To mitigate the LC, the NPC DC decoupling method is introduced [6]. The method utilizes additional inductors and a modified modulation strategy to achieve a balanced current flow in the NPC capacitors. By controlling the voltage across the NPC capacitors, the LC is minimized, improving the overall performance of the multilevel inverter. The method significantly reduces the LC compared to conventional control strategies, improving power quality and increasing system efficiency. The DC decoupling three phase three leg TLPV inverter topology [7] with its associated techniques presents an efficient approach to reducing LC, managing terminal pole voltages during the common zero state, and minimizing CMV variations. These advancements improve power quality, reliability, and performance in PV systems. In Pulse Width Modulation (PWM) techniques, carrier and modulation [8] based PWM techniques are popular in multilevel inverters (MLI) to reduce switching loss, eliminate CMV, lower neutral point fluctuation and DCL balancing for the desired voltage requirements. The CMV in PV systems can lead to LC, which poses safety concerns and reduces the insulation lifespan and failure of bearings in motor drive systems in industrial applications. A zero CMV PWM and its hybrid PWM [9] can be used to eliminate LC in NPC inverters to address the issue of CMV, LC, and neutral-point (NP) voltage imbalance. A Pulse Width Modulation (PWM) Zero Voltage Switching high-frequency-link three-phase inverter with a T-Type NPC unfolder [10] provides reduced switching losses and improved efficiency, and a balanced output voltage with reduced harmonic distortion. This configuration helps to improve the overall power quality of the inverter system. ZVS allows for soft switching of the power devices, minimizing the stress on the semiconductor devices and improving their lifespan.

One-cycle control-based Pulse Width Modulation (PWM) method [11] offers several advantages, including low cost, simple implementation, a constant switching frequency, enable bidirectional power flow and with unity power factor proposed. It ensures stable operation of the 3L-NPC converter even under sudden load changes or when operating in inverting mode. The low voltage network-based grid converter-based devices and multiple feedback loop voltage control strategies introduce new challenges, such as stability and harmonic oscillations controlled by the smart transformer fed [12] distribution grid. The challenges faced by the electric grid when integrating renewable energies and electric vehicle charging stations. The smart transformer [13] can better manage the system’s interdependencies, optimize its operation, and improve grid stability by acting as a centralized control point. The Scott-transformer-based power factor-controlled rectifier combined with the three-level NPC inverter-fed induction motor drive system,[14] enhanced by the current feed forward control scheme and using a space vector-modulated indirect vector control scheme, offers improved power quality and dynamic performance. It is observed that the proposed system exhibits a faster response with reduced overshoot and undershoot. Deadbeat predictive control [15] is a control strategy that aims to eliminate control errors within a predetermined number of switching periods and its advantages in achieving precise control and excellent dynamic performance. Model predicative control is a control strategy that uses a mathematical model of the system to predict future behavior and optimize control actions accordingly. The utilization of deadbeat predictive control in conjunction with modulation, predictive current control that offer precise control, improved dynamic performance, and effective regulation in different applications.

A hybrid strategy called selective harmonic mitigation pulse width modulation (PWM) [16] for reducing the common-mode voltage in a Three-Phase Three-Level NPCI. This technique is also employed to eliminate specific low-frequency harmonics, while the PWM technique is used to regulate the fundamental voltage. Combining these techniques allows the inverter to reduce the common-mode voltage while maintaining the desired output voltage quality. For single-phase topologies, examples such as H5, oH5, and H6 are mentioned, which are techniques designed to mitigate LC. However, it is noted that the VDE 4105 standard limits the capacity of single-phase grid-connected inverters to less than

4.6 kVA.[17] The Z-source inverter is a unique topology known for its ability to handle various power conversion requirements. In this case, it is employed in a PV system to address the challenge of LC. The advantages of the Z-source four-leg inverter include unbalanced operation, fault tolerance capability, high reliability, and absence of dead-time requirements or risks of overcurrent due to leg short circuits. Therefore, there is a need for further exploration and research to develop new solutions for LC reduction in Z-source three-phase four-leg inverters. A specific type of multilevel inverter called a Five-Level quasi-Z-source based NPCI [18] for photovoltaic (PV) applications. To achieve high boost gain and reactive power capability, the inverter utilizes level shifted pulse width modulation with a hybrid shoot-through technique. This modulation technique allows for precise control of the output voltage and reactive power, enhancing the performance of the inverter. A three-level neutral point clamped structure with an inductor-capacitor switching network.[19] This LC network boosts voltage by storing and releasing energy during switching. Incorporating the Three-Level LC-Switching-Based Voltage Boost allows NPCI to achieve high voltage gains for various applications, such as renewable energy systems and maintain stable operation. Fast capacitor voltage balancing in a three-level NPC inverter ensures stable operation and optimal inverter performance. The proposed modulation strategy focuses on achieving fast capacitor voltage balancing [20] by actively redistributing the charge between the capacitors. The compensator is designed to generate optimal compensation coefficients and offset signals using PSO optimization. This is accomplished by introducing additional switching states that facilitate charge transfer between capacitors during modulation. MPPT is a technology used in PV systems to ensure that the solar panels operate at their maximum power output by continuously tracking and adjusting the operating point of the panels. There are several MPPT techniques available, each with its advantages and disadvantages [21].

A direct power control (DPC) strategy is developed to infuse generated solar energy into the electrical network. This injection aligns with a reference design aimed at eliminating reactive power and harmonics originating from nonlinear loads. [22]. This article provides explanations of these renewable energy sources, Maximum Power Point Tracking (MPPT) techniques, and hybrid systems. [23]. Model for a microgrid featuring a solar power system with maximum power point tracking (MPPT) and a battery energy system is presented. A Boost converter is utilized to match the voltage level with the MPPT [24]. Boosting the power capacity of the current grid system and integrating renewable energy sources are essential. Consequently, this study tackles the necessity of employing intelligent techniques to effectively link renewable energy sources to the grid. [25]. This article introduces an elaborate computational model for organic photovoltaic (OPV) cells, specifically based on a single-diode framework. These cells utilize organic semiconductor materials, offering advantages in terms of cost and weight compared to traditional PV cells. [26].

1.2 Contributions

The proposed work was developed for a grid-connected system to achieve the following objectives.

- To eliminate the effect of common mode voltage (CMMV) and leakage currents (LC) in the three-phase transformerless grid connected neutral point clamped inverter, and transformerless T-type four leg grid connected neutral point clamped inverter.
- The DC link balance is maintained using an ANN controller, resulting in a shorter settling time compared to a standard PI controller.
- Implementation of 4-leg T-Type NPC with SVPWM control technique to interface with the three-phase grid synchronization and to mitigate CMMV, LC effectively. The results are compared with the conventional three phase NPCI.
- THD of grid current is minimum with ANNC as compared with PIC.

1.3 Organization of the Paper:

The proposed paper focuses on the analysis of ANNC for a T^{3}LGC-NPCI. Section 2 provides details about the TLGC-NPCI and T^{3}LGC-NPCI configurations, PV system including with design of DC-link capacitor, filter and grid synchronization. In Section 3, ANNC, SVPWM techniques, CMMV and LC are discussed. Finally, Section 4 presents the simulation results.

2. Proposed Configuration:

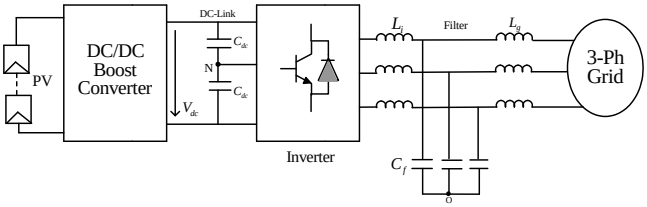


Fig.1. Block diagram of Grid Connected Solar PV System

The structure of the solar grid connected inverter is shown in Fig.1. The dc side of inverter is connected to the PV via DC-DC boost converter. TL inverters are favored in PV grid-tied systems due to their advantages such as increased efficiency, reduced cost, and compact size. However, it's important to note that these inverters lack galvanic isolation, which results in higher LC compared to isolated inverters. This increased LC leads to several issues, including elevated EMI, greater total THD, higher system losses, and safety concerns.

2.1 T^{3}LGC-NPCI:

Fig.2 shows a three phase three leg NPCI configuration consisting of two capacitors on the DC side. This configuration allows for the generation of three-level phase voltages on the AC side. However, it is important to note that imbalances in the capacitor voltages can have an impact on the

AC side voltages, potentially causing unexpected effects on various system parameters.

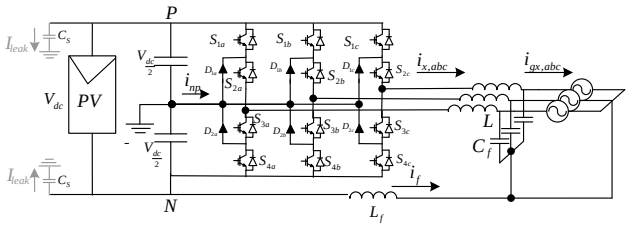


Fig.2. Three-Phase Three-Level TL Grid Connected NPC Inverter

The phase leg-A of the inverter comprises four IGBT switches (S1a to S4a) and their respective anti-parallel diodes. The neutral point (N) is established between two series-connected capacitors. Additionally, clamping diodes (D1a and D2a) are connected to the neutral point to provide clamping functionality. Table 1 presents the switching states of the NPCI along with the corresponding output voltage. Depending on the specific switching state and the direction of load currents, the neutral current (i_N) can either charge or discharge the capacitors, resulting in an imbalance in the neutral-point voltage (NPV).

Table.1 Switching states of TLGC-NPCI

Switching States (S_A)	switching status (Phase A)				Inverter terminal Voltage V_{AC}
	S_1	S_2	S_3	S_4	
2	ON	ON	OFF	OFF	$V_d/2$
1	OFF	ON	ON	OFF	0
0	OFF	OFF	ON	ON	$-V_d/2$

2.2 T³LGC-NPCI:

The NPC inverter necessitates four IGBTs and six diodes in each phase, with a breakdown voltage equal to half of the DCL voltage (V_{dc}). In this configuration, two IGBTs actively conduct current in each phase simultaneously. In contrast, the T-type NPC, derived from the three phase three leg NPCI, requires four diodes in each phase. However, only one IGBT conducts current in each phase leg at any given time, resulting in lower conduction losses. Consequently, the T-type NPCI proves to be more efficient than the diode-clamped NPC at medium switching frequencies. Fig.3.shows the three-Phase Four Wire Three-Level T³L Grid Connected NPC Inverter and the ratings and specifications of proposed system is given in Table.3.

Nevertheless, in the T-type NPCI, the switching losses of the outer switches are relatively higher. This occurs because SW_{1a} and SW_{2a}, along with their freewheeling diodes, block the full DCL voltage. As a consequence, the efficiency of the T-type NPC reduces as the switching frequency increases.

When both switches SW_{2a} and SW_{3a} are turned off simultaneously while SW_{1a} is on, the output voltage will be positive [P]. Similarly, deactivating SW_{1a} and SW_{2a} and turning on SW_{3a} will result in the neutral voltage level [O]. Turning off SW_{1a} and SW_{3a} and activating SW_{2a} will generate the negative voltage level [N] and its switching states is shown in Table.2. It is important to note that the current follows the appropriate path regardless of its direction. To avoid any potential DC bus short circuit, a dead time is incorporated for all switches. This dead time ensures that there is a brief interval during which both switches are off before changing states to prevent any harmful electrical effects.

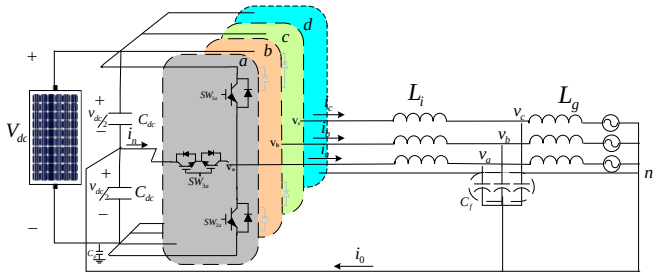


Fig.3. Three-Phase Four Wire Three-Level T³L Grid Connected NPC Inverter

Table.2 Switching states of T³LGC-NPCI for leg A

Switching States	S_{1a}	S_{2a}	S_{3a}	V_{AC}
+1	ON	OFF	OFF	$V_{dc}/2$
0	OFF	OFF	ON	0
-1	OFF	ON	OFF	$-V_{dc}/2$

2.3 PV System (PV):

To achieve the required voltage and current levels, the PV cells are connected in series to form a string. Multiple strings are then connected in parallel. In the module, every PV cell is modeled by a diode in parallel with the current source as shown in Fig 4. The model of the PV system with a boost converter is shown in Fig.5.

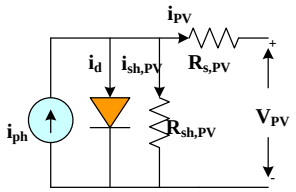


Fig 4. PV cell model

It having of a photo current source (i_{ph}) with a forward diode carrying current (i_d), a series, and parallel cell resistances ($R_{s,PV}$ and $R_{sh,PV}$) carrying a current of (i_{PV}, $i_{sh,PV}$). The PV cell identifies sun irradiation and converts it into current. By adopting KCL, PV cell output current (i_{PV}) is obtained by Eq. (1)

$$i_{PV} = i_{ph} - i_d - i_{sh} \quad (1)$$

By, substituting expressions for i_d, i_{sh} , the PV module output current is obtained is given by Eq. (2)

$$i_{PV,m} = i_{ph} - i_{S,PV}[\exp(\frac{Q(V_{PV} + (i_{PV,m}R_{S,PV}))}{\eta k T_C}) - 1] - \frac{V_{PV,m} + (i_{PV,m}R_{S,PV})}{(R_{sh,PV})} \quad (2)$$

Where, $i_{PV,m}$, $V_{PV,m}$ is the module current and voltage, $i_{S,PV}$ is the reverse saturation current, Q is the electron charge,

η is the diode ideal factor, k Boltzmann's constant, and T_C denotes the cell temperature, and N_s is series connected PV cell. Fig. 6 and 7 illustrates the PV and IV characteristics of a SPV system under different temperature and solar irradiation conditions. The PV modules are connected in series and parallel to form an array by Eq. (3)

$$i_{PV,m} = i_{ph}N_p - i_{S,PV}N_p[\exp(\frac{Q(V_{PV} + N_s/N_p(i_{PV,m}R_{S,PV}))}{N_s\eta kT_C}) - 1] - \frac{V_{PV,m} + N_s/N_p(i_{PV,m}R_{S,PV})}{N_s/N_p(R_{sh,PV})} \quad (3)$$

Where,

$$i_{ph} = (i_{ph,n} + K_1\Delta T_C)\frac{G}{G_n} \quad (4)$$

Where, G, G_n represents solar irradiance (W/m^2) and at STC, ΔT_C variation in temperature. The output power of PV ($P_{PV\max}$) is calculated by Eq. (5).

$$P_{PV\max} = V_{PV\max} \times i_{PV\max} \quad (5)$$

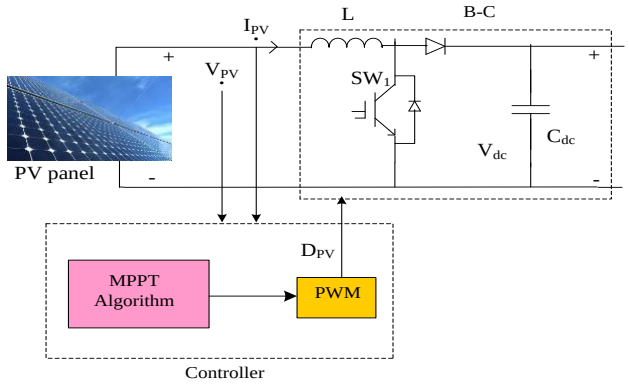


Fig.5 PV system

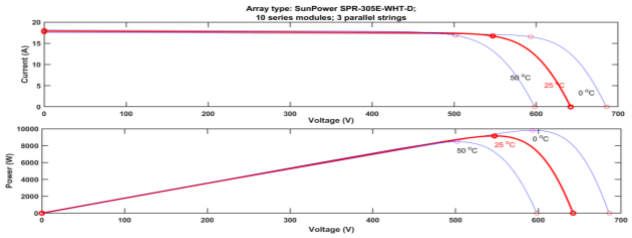


Fig.6. PV Array I-V and P-V waveforms at different temperatures

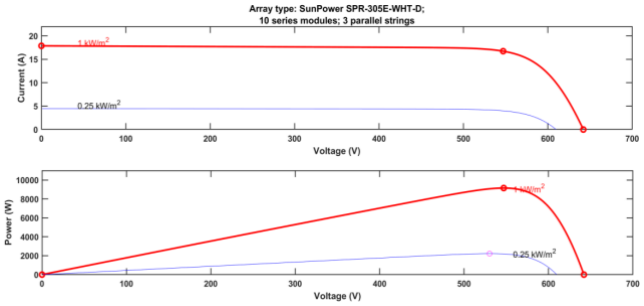


Fig.7. PV Array I-V and P-V waveforms at different irradiances

Table.3 Proposed System Specifications

S.no	Parameters	Values
1	Maximum power of PV module (Strings: series =10, parallel =3)	5 kW
2	Boost converter Inductance	1.45 µH
3	Boost converter Capacitance	3227 µF
4	Boost converter output voltage	700 V
5	DCLink bus capacitance	4,667 µF
6	Pre charging circuit resistance	200 Ω
7	Inverter switching frequency	5 kHz
8	Filter Inductance	1.79 mH
9	Filter capacitance	100.28 µF
10	PLL-PI controller Kp,Ki values	10,50000
11	Grid voltage Vrms	415 V
12	Grid Frequency	50 Hz
13	Grid internal resistance, Inductance	5.6 Ω,0.65 mH

2.4 NPV controller

The role of the DCL voltage controller is to maintain the DCL capacitor voltage at a desired level, as determined by the reference voltage V_{dc_ref}. This reference voltage is typically determined by the MPPT scheme, which optimizes power generation. To achieve proper regulation of the DCL voltage, the controller adjusts the direct axis current. By controlling this current, the controller effectively governs the real power injection into the grid. In essence, the DCL voltage regulation is accomplished by managing the direct axis current, which in turn influences the amount of power that is fed into the grid.

$$V_{dc} = \frac{2\sqrt{2}VLL}{\sqrt{3}m} = \frac{2\sqrt{2}}{\sqrt{3}}\frac{VLL}{m} = 1.633\times\frac{415}{1} = 677.69 \text{ V} \quad (7)$$

Where m is the modulation index considered as 1, hence $V_{dc} \cong 700$ V. The capacitor value is decided by maximum active power to be handled under load transients. For full cycle T = 20 msec and for half cycle T = 10 msec.

2.5 Capacitor value of DC-Link

The equation for the DCL capacitor is presented as follows:

$$V_{dc,\min} = \frac{3V_{ph}ia_f k_e t}{1/2(V_{dc}{}^2 - V^{ref}{}_{dc}{}^2)} \quad (8)$$

Based on the given parameters, the minimum calculated voltage of the DCL capacitor is as follows 677.69V, while the maximum voltage is 700V. The calculated current is 230.9A, and the time duration is 30ms. The energy variation during dynamics is 10% (0.1). The measured value of the capacitor (C) is 9330.2µF, which is approximated as 9400µF. To achieve this value, two split capacitors are used, with each capacitor set to 4700µF.

2.6 Inductor Ripple Filter

The passive filter is connected to the network via an inductor and relies on parameters such as the switching

frequency, ripple current, and DCL voltage. The equation for the interfaced inductor is presented as follows:

$$L = \frac{\sqrt{3}(m)(V_{dc})}{12(a_f)(f)(I_{cr,pp})} \quad (9)$$

Here, the ripple current for the inductor is measured to be 20% of the root mean square (rms) phase current of the Active Power Filter (APF). Considering $I_{cr,pp} = I_r$ =20%, f =10 kHz, m =1, V_{dc} =700V, and a_f =1.5, the value of L is measured as 1.79mH.

2.7 Grid Synchronization

Grid synchronization is a vital requirement for a grid-tied converter, and it is commonly accomplished using a PLL. The PLL plays a crucial role in synchronizing the converter with the grid by transforming the three-phase voltages into the d-q axes. By utilizing the filtered grid voltages, the PLL enhances the accuracy and effectiveness of synchronization. Inverters equipped with a DCL capacitor connected to PV system possess the capability to offer reactive power to the grid as an ancillary service. This additional functionality allows the inverter to contribute not only to real power generation but also to the provision of reactive power, which supports grid stability and performance.

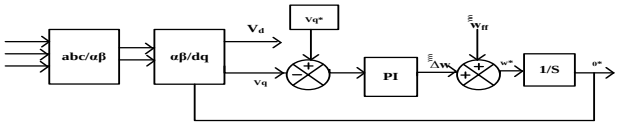


Fig.8. Synchronous Reference Frame (SRF) based PLL

In order to achieve synchronization, accurate determination of the phase angle and amplitude of the utility grid voltage is essential. This is accomplished by utilizing Park's transformation to convert the three-phase electrical quantities into d-q axis quantities. To execute this task, a SRF approach is employed, incorporating a PLL shown in Fig.8. The utility grid voltage, represented as V_{abc}, undergoes a low-pass filtering process. The filtered voltages are then transformed into d-q axis quantities, while the PLL is responsible for determining the phase angle accurately. By employing this approach, synchronization with the utility grid is achieved effectively.

3 Control Technique

3.1 ANN Controller

ANN is the trending intelligence controller whose work is inspired by the behavior of the human brain with the advantage of self-adapting unique techniques. Multilayer perceptions (MLP) are famous in ANNC. Therefore, it is very suitable for power controllers. The structure of ANNC contains an input layer (IL), a hidden layer (HL) and an output layer (OL) shown in Fig.9. The input data is stored in IL and moves to HL. Later, it multiplies with weights on the links, which are present between IL and HL. Usually, calculations are done in HL, whereas OL gives the results.

In the MLP structure, neurons are interlinked between the layers with their numerical weights, where each neuron possesses both the summation function (SF) and activation functions (AF). The necessity of SF is to add up the product of input and weights with bias as shown in Eq. (11), where w_{pk} is the weight from p to neuron k; β_k is a bias for k^{th} neuron; and m is the total number of inputs. In this work nonlinear sigmoid function is used given in Eq. (11). The output of a k^{th} neuron is given in Eq. (12).

$$S_k = \sum_{p=1}^{m} w_{p_k} I_p + \beta_k \quad (10)$$

$$f(x) = \frac{1}{1+e^{-x}} \quad (11)$$

$$O_k = f_k\left(\sum_{p=1}^{m} w_{p_k} I_p + \beta_k\right) \quad (12)$$

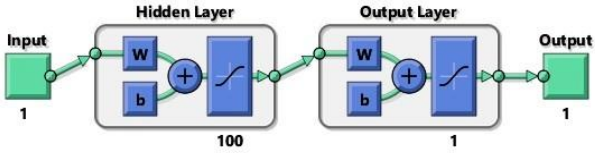


Fig. 9. Structure of ANNC

In this work, Feed-forward artificial neural network is adapted to obtain the constant DCL voltage across microgrid. During the training the link of weights is updated automatically. The training process is carried out to minimize errors and obtain the desired output.

By analyzing the regression plot displayed in Fig. 10 and taking into account the co-relation co-efficient value (R), it becomes evident that the FFNN has been successfully trained using the provided training datasets. The testing, validation, and overall system performance are also deemed satisfactory. An R value of 1 indicates perfect correlation.

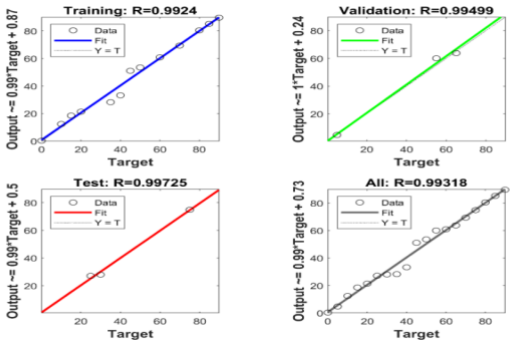


Fig.10. Regression plot of ANN controller

3.2 SVPWM Modulation Method

Fig.11 depicts the space vector diagram of a three phase three leg NPC inverter. The space vector plane is divided into six sectors, each of which is further subdivided into four subsectors. In contrast to a two-level inverter, the three-level inverter provides three distinct voltage states: $+V_{dc}/2$, 0, and $-V_{dc}/2$. These voltage states do not have equal magnitude voltage vectors. As a result, they are categorized into four types based on their magnitudes: zero vectors (with a magnitude of 0), 12 small vectors (with a magnitude of

$0.334V_{dc}$), 6 medium vectors (with a magnitude of $0.577V_{dc}$), and 6 large vectors (with a magnitude of $0.667V_{dc}$).

In Fig.12, the proposed controller's Switching pattern using SVPWM is presented. The three-level inverter is composed of a total of 27 switching states, which allow for the selection of 19 distinct voltage vectors. The voltage vectors in the inverter can be categorized into five groups, depending on their amplitudes and how they affect the capacitor voltages on the AC side. These groups are: zero vectors, Three (000, 111, and 222), long vectors, Six (200, 220, 020, 022, 002, and 202), medium vectors, Six (210, 120, 021, 012, 102, and 201), upper short vectors, Six (211, 221, 121, 122, 112, and 212), lower short vectors, Six (100, 110, 010, 011, 001, and 101).

These categorizations are based on the magnitudes of the voltage vectors and their impact on the capacitor voltages within the inverter's AC side. However, restricting the switching states solely to achieve zero CMV can hinder the inverter's ability to synthesize an output voltage that closely resembles a sinusoidal waveform. Therefore, it is crucial to minimize the magnitude of the CMV in order to minimize adverse effects and ensure smooth operation. To achieve this goal, voltage vectors that result in both zero CMV and $V_{dc}/6$ are selected. By choosing these specific voltage vectors, the inverter can achieve the objective of minimizing the CMV magnitude while maintaining a waveform that closely resembles a sinusoidal shape. Table.4 shows switching time calculation of Vref vector in sector-I

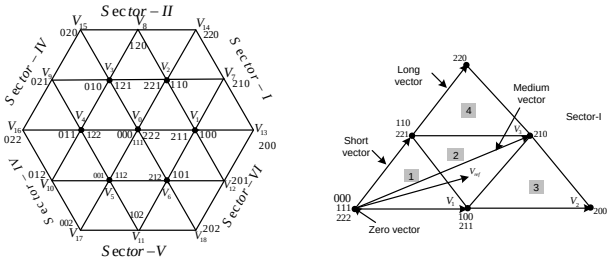


Fig.11. State space vector structure and regions representation in sector-I of three phase three leg NPCI

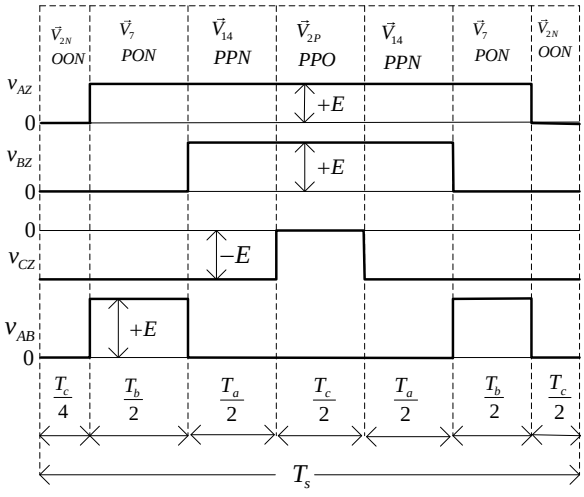


Fig.12. Switching pattern using SVPWM

Table.4 Dwell Time Calculation for V_{ref} in Sector-I of 3P-3L NPCI

Reg	T_a		T_b		T_c	
1	$\vec{V}_1$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$\vec{V}_0$	$T_s\left[1-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$\vec{V}_2$	$T_s[2m_a\sin\theta]$
2	$\vec{V}_1$	$T_s[1-2m_a\sin\theta]$	$\vec{V}_7$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$	$\vec{V}_2$	$T_s\left[1-2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$
3	$\vec{V}_1$	$T_s\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$\vec{V}_7$	$T_s[2m_a\sin\theta]$	$\vec{V}_{13}$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$
4	$\vec{V}_{14}$	$T_s[2m_a\sin\theta-1]$	$\vec{V}_7$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$\vec{V}_2$	$T_s\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$

3.3 Common Mode Voltage (CMV) in 3P-3L NPCI

The CMV is characterized as the voltage disparity between the midpoint of the DCL capacitor and the load's neutral point and it is depicted in Fig.13.

$$V_{cmv} = 1/3(V_a + V_b + V_c) \qquad (13)$$

The pole voltages Va, Vb, and Vc represent the voltages of phases A, B, and C, respectively. In both two-level and three-level inverters, the CMV does not sum up to zero, resulting in the generation of high-frequency CMV in the motor winding. Higher CMV levels lead to common-mode current (CMC) and other undesirable issues. To address this problem, numerous modulation techniques have been proposed to reduce the CMV to acceptable levels. These techniques aim to minimize CMV and mitigate its potential adverse effects.

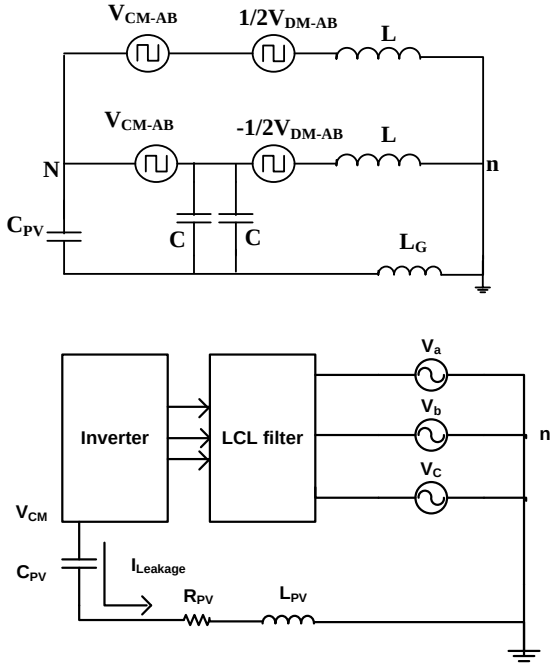


Fig.13. Representation of CMV and LC in proposed system

3.4 Leakage current in three phase three leg NPCI

The presence of CMV variations in a three-level converter can lead to LC in the line current. In the context of a three-phase motor drive system, CMV induces LC that flow to the ground. This LC in motor drive applications causes additional harmonics, energy losses, EMI, and potential safety concerns. For instance, high-frequency LC can trigger

malfunctions in ground relays, posing risks to the motor drive system.

PWM inverters commonly used in motor drive applications also introduce CMV from the neutral point of the three-phase winding to the ground. This results in LC flowing through parasitic capacitance between the stator winding and the motor frame, further contributing to potential issues.

In 3P-3L NPCI systems, the LC caused by CMV can lead to potential induced degradation (PID) of PV panels.

The LC is directly proportional to C_{SPV}, and variation in CMV is expressed as

$$i_{leakage} \propto C_{PV} \frac{dV_{CMV}}{dt} \quad (14)$$

The stray capacitance C_{PV} typically ranges from 7nF to 1μF per kilowatt. The exact value depends on factors such as the material, type of PV module, and prevailing weather conditions.

LC in PV systems are high-frequency components resulting from the continuous switching of the inverter. These LC have implications for the quality of the output power. They can couple with the grid current, leading to increased THD, losses, and EMI. The presence of LC can impact the overall operation of the inverter and compromise personal safety. Table.5, shows the limits specified by German standard DIN VDE 0126-1-1

Table.5 LC Limits

Average LC (mA)	30	60	100	300 (peak)
Time limit (sec)	0.3	0.15	0.04	0.3

4. Simulation Results

The proposed TLGC-NPCI and T^{3}LGC-NPCI were developed in MATLAB Simulink environment given in Fig.14 and Fig. 15 respectively. The sub system diagram for solar is exhibited in Fig. 16. The grid voltage and current waveforms, the LC and common mode voltages were analyzed. In addition, the THD was obtained for the proposed system and further, it is compared with PI controller, as illustrated in Table.5.

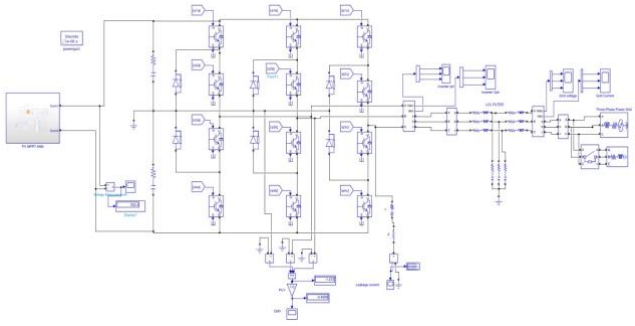


Fig.14 Matlab/Simulink diagram of proposed TLGC-NPCI

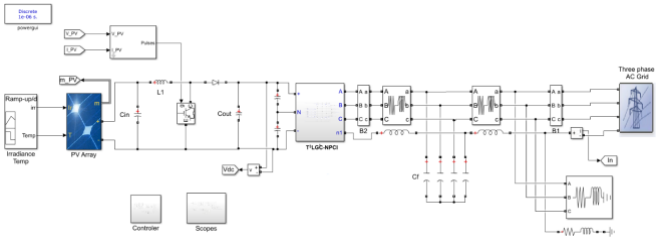


Fig.15 Matlab/Simulink diagram of proposed T^{3}LGC-NPCI

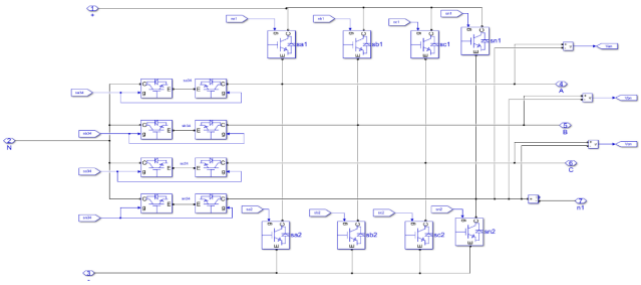
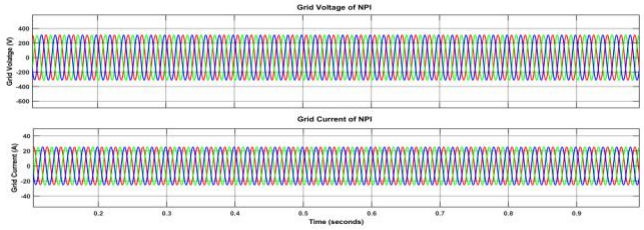


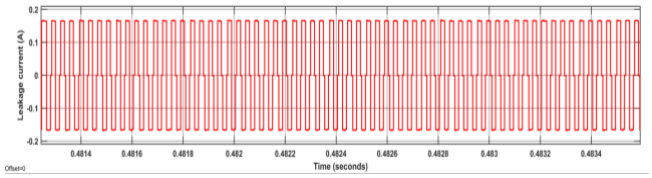
Fig.16 Sub circuit of T^{3}LGC-NPCI

In Fig. 17(a), the sinusoidal form of the grid voltage and current is depicted, with magnitudes of 380V and 24A, respectively. The waveform for LC and CMV for the proposed TLGC-NPCI is illustrated in Fig. 17(b) and 17(c). Moving on to Fig. 18(a), it showcases the grid voltage and current waveforms, with magnitudes of approximately 380V and 20A. Meanwhile, Fig. 18(b) and 18(c) display the LC and CMV waveforms for the proposed T^{3}LGC-NPCI, respectively. It can be observed that from both Fig. 17 and Fig. 18, the incorporation of the fourth leg effectively reduces the magnitudes of LC from 180mA to 30mA and CMV from 360V to 220V. The line-to-line voltage waveform for leg A of the proposed inverter configuration is as shown in Fig.19. Fig.20 illustrates that the grid voltage and current are in phase, which shows the power factor is maintains as Unity.Fig.21 displays the required pulses generated by the SVPWM technique for the proposed 3P-3L NPCI of leg A, while the corresponding sector waveform is provided in Fig.22.

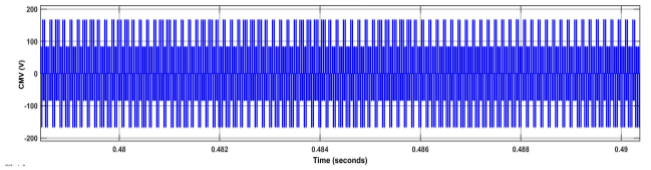
Furthermore, Fig.23 and 24 shows the DCL voltage waveform under various solar irradiation values and at a constant temperature, using PI and ANN controllers. It is evident that the ANN controller achieves a faster settling time, resulting in a constant voltage across the DCL. The THD spectrum for grid current with PI and ANN controllers is as shown in Fig.25 and 26 respectively. It can be evident that the THD with ANN controller is less compared to the PI controller for the proposed system. The comparison table for LC and CMV is given in Table.6.



(a)

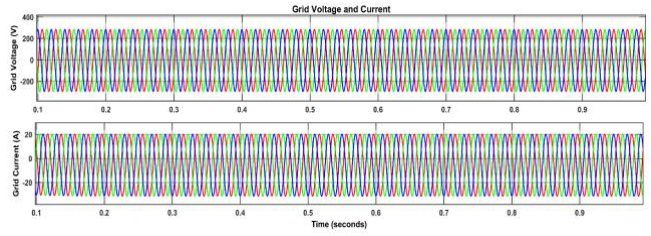


(b)

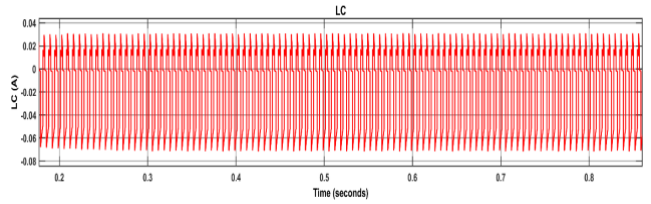


(c)

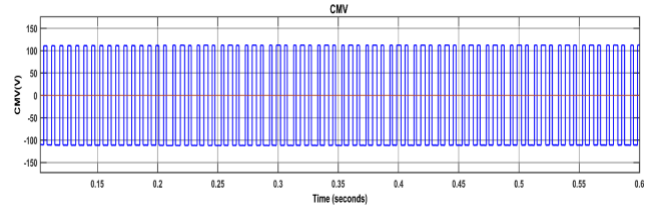
Fig.17. (a) Output Grid Voltage and Grid Current waveforms (b) Waveform for LC (c) CMV generated by SVPWM technique for GCTL-NPCI



(a)



(b)



(c)

Fig.18. (a) Output Grid Voltage and Grid Current waveforms (b) Waveform for LC (c) CMV generated by SVPWM technique for GCT^{3}L-NPCI

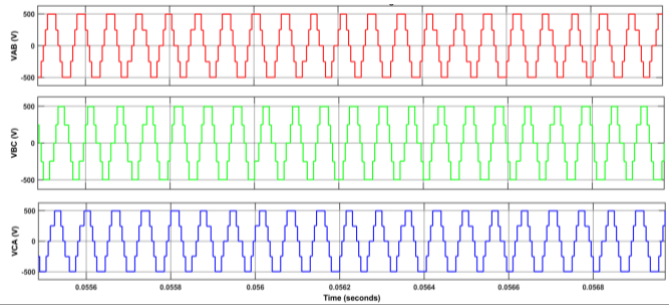


Fig.19. Output line-line voltages

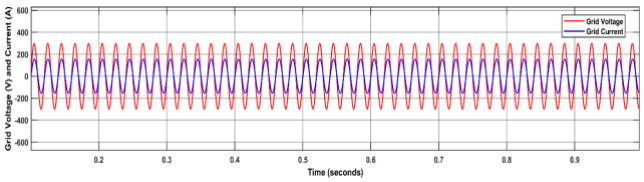


Fig.20. Waveform of UPF

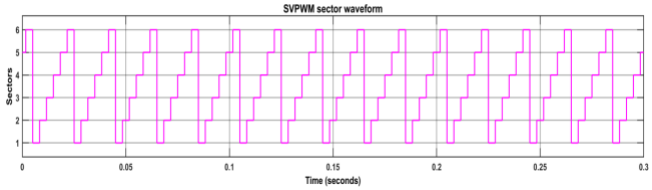


Fig.21. Sector Generation by SVPWM

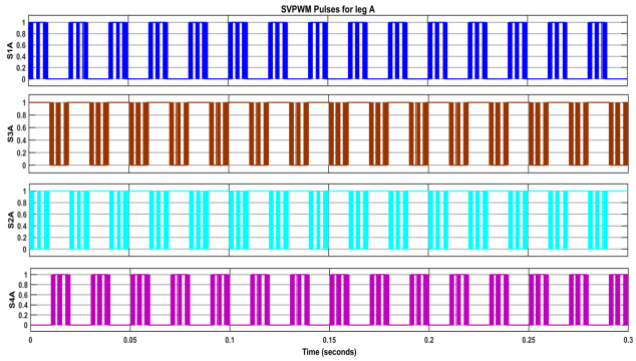


Fig.22. SVPWM pulses

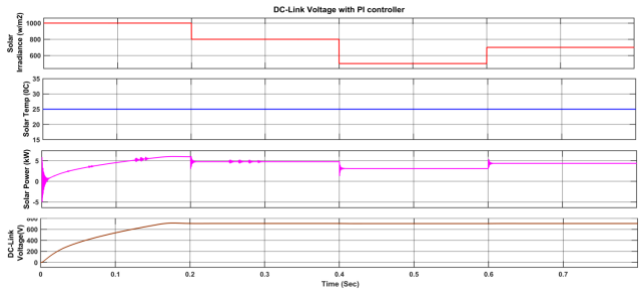


Fig.23. DCL voltage waveform at different solar irradiances of proposed configuration using PI controller

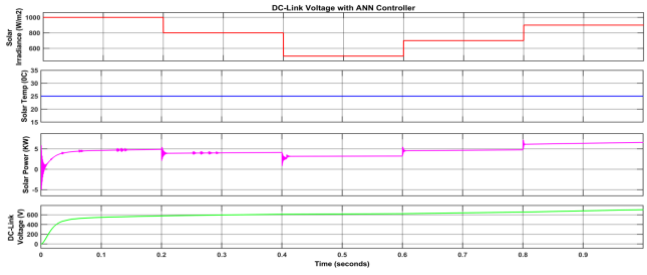


Fig.24. DCL voltage waveform at different solar irradiances of proposed configuration using ANN controller

Table. 6. Comparison table for LC and CMV

Parameter	With existed configuration	With proposed configuration
LC (mA)	160	30
CMV (V)	300	220

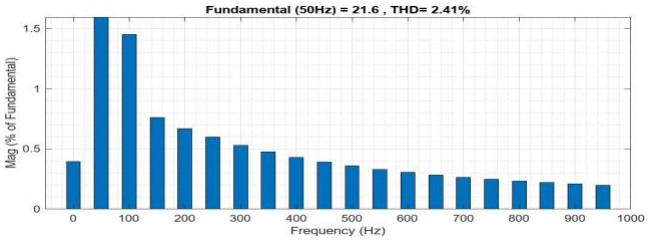


Fig.25. Grid current THD using PI control

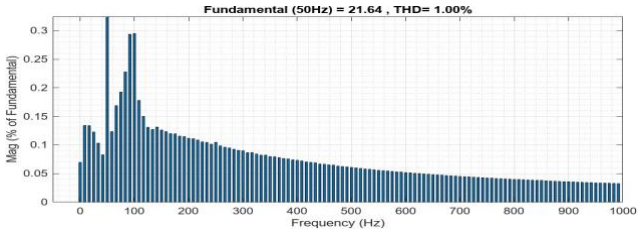


Fig.26. Grid current THD using ANN control

5. Conclusion

In this article, we introduced a novel configuration that incorporates a T-type four-leg NPCI. This configuration effectively reduces both Common Mode Voltage (CMMV) and Leakage Current (LC), while also minimizing the number of switches required in comparison to the TLGC-NPCI. These features make it highly suitable for grid-connected applications, ensuring safe and reliable operation for generating pulses using the Space Vector Pulse Width Modulation (SVPWM) technique.

Furthermore, we integrated an Artificial Neural Network (ANN) controller with the SVPWM technique in the proposed configuration to maintain a constant voltage across the DC Link (DCL) under varying solar irradiation and temperature conditions. This integration resulted in high-quality inverter-side output currents with low Total Harmonic Distortion (THD). Significantly, the ANN controller demonstrates its superiority in DCL voltage regulation by achieving a faster settling time compared to the conventional Proportional-Integral (PI) controller.

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