Model Predictive Control for Current Balancing in a Four-Phase Buck Converter

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Received: 25.02.2016 Accepted: 07.05.2016

Abstract-Multiphase buck topology offers smaller ripple current and lower component ratings. This, however, compromises unbalanced output current between each phase of an inductor which leads to over-current and inductor saturation issues. Often when discussing the linear control schemes, it involves the use of superposition theorem to understand the system's response. However, the limitation of superposition theorem in this application is that it assumes the circuit to be completely linear. For components with nonlinear behaviour such as power switches and diodes, the analytical results may not be accurate resulting to unexpected behaviour as the algorithm is implemented on a real system. Hence, the use of a more advanced control scheme is necessary to improve a system with a non-linear characteristic. This paper proposes a current limit control (CLC) consists of MPC for inner loop control and PID for outer loop control for phase current balancing in a four-phase buck converter. The controller is designed to achieve balanced current for each phase with acceptable response time. The proposed system is designed using MATLAB/Simulink simulation software and verified by a laboratory prototype with a TMS320F28335 as the main controller. Simulation and experimental results are provided to validate the system performance.

Keywords-Buck Converter, multiphase DC-DC, Current Controller, Lithium-ion battery, Renewable Energy.

1. Introduction

Multiphase step-down converter is a switch-mode power supply in which consists of MOSFET, inductor, capacitor, and a diode. Its main function is to regulate the output and offers many advantages under interleaved operation [1-3]. Perhaps the most significant features of this parallel connected topology are it allows the use of smaller rated devices for a high-current application. Furthermore, this topology easily allows future expansions (by adding additional N circuit in parallel) to enhance the system's overall performance [1]. Conventionally, output regulation for a single-phase buck converter was achieved using peak current mode (PCM) or average current mode (ACM) [2, 3]. PCM simply compares the output error with peak inductor current to control its duty cycle. This method, however, is likely to be unstable if it operates beyond 50% of a duty cycle. Thus, a slope compensator is usually added to improve this problem. ACM, on the other hand, is an improvement made to solve certain issues at PCM [4].

Due to the parallel connected structure of a multiphase, balancing control is required to ensure equal current distribution among phases. A small difference in current of each phase (millivolts) will lead to operation beyond the inductor's limit or inductor saturation. There are few balancing schemes that had been proposed in Reference [5-6], i.e. passive and active current scheme and the conventional droop method. The passive droop method is easy to implement as it works only by adjusting the DC gain of a control loop and does not require any additional control circuit. Droop method has a low accuracy of output in which unacceptable for certain applications. An Active current scheme such as master-slave control (MSC) requires one phase to be assigned as a master while the others are the slave. The output current of each slave will be forced to follow the master, thus achieving balanced current sharing in each phase.

A digitally controlled sliding-surface was proposed for a two-phase parallel DC-DC buck converter [7]. The controller shows excellent steady state response under fixed switching frequency. However, the experiment was demonstrated for a two-phase system with fixed resistive loss. With fixed resistive loss, the control capabilities for dynamic system's response cannot be completely evaluated. A hysteresis based controller was proposed for a buck converter in [8] where the

reference signal was compared directly with the feedback signal, the error signal was then controlled to be in the upper-limit and lower-limit which then determine the switching state.

Exclusive nonlinear modelling such as switching dead time, on/off delays, semiconductor behaviours, and external disturbances are the common causes of unstable operation in controllers [9-11]. The control schemes depend very much on the poles and zero placement of the system transfer function. The number of poles and zeros increase with the increase of plant transfer function order. Practical design for the controller becomes complex and the stability of the system becomes limited.

This paper proposes a current limit control (CLC) consists of MPC for inner loop control and PID for outer control for phase current balancing in a four-phase buck converter. The controller is designed to achieve balanced current for each phase with acceptable response time. The performance of the proposed system is evaluated based on i) step resistive load, ii) step output current, and iii) variable input sources using lithium ion battery as the load. In Section 2 and 3 describes the working principle of the proposed system. The simulation result of multiphase buck converter comprises the proposed inner-loop and outer loop control and also the conventional CLC are presented and compared in Section 4. The design verification is carried out in Section 5. Finally, the conclusion is presented in section 6.

2. Configuration of State Model

Fig. 1(i) shows the conventional CLC current balancing control scheme for each phase inductor configuration. The configuration consists of an inner-loop, where each phase inductor is responsible for its current regulation and the outer-loop which functions to determine the error signal ΔI1(s):

$$\Delta I1(s) = Iref(s) - io(s) \times H1(s) - iL1(s) \times H2(s) \quad (1)$$

Here, H1(s) and H2(s) are sensor gains for the output current, inductor current iL1 and inductor current iL2, respectively. The relationship between the input and output of each phase inductor can be expressed as:

$$iL1(s) = \frac{\mathrm{E}(s)/ZL1}{1+T1} - \frac{Vc(s)/ZL1}{1+T1} \quad (2)$$

$$iL2(s) = \frac{E(s)/ZL2}{1+T2} - \frac{Vc(s)/ZL2}{1+T2} \quad (3)$$

The loop gain T1 and T2 are expressed as Eq. 4.

$$T1 = \frac{H2(s)}{ZL1} \;;\; T2 = \frac{H3(s)}{ZL2} \quad (4)$$

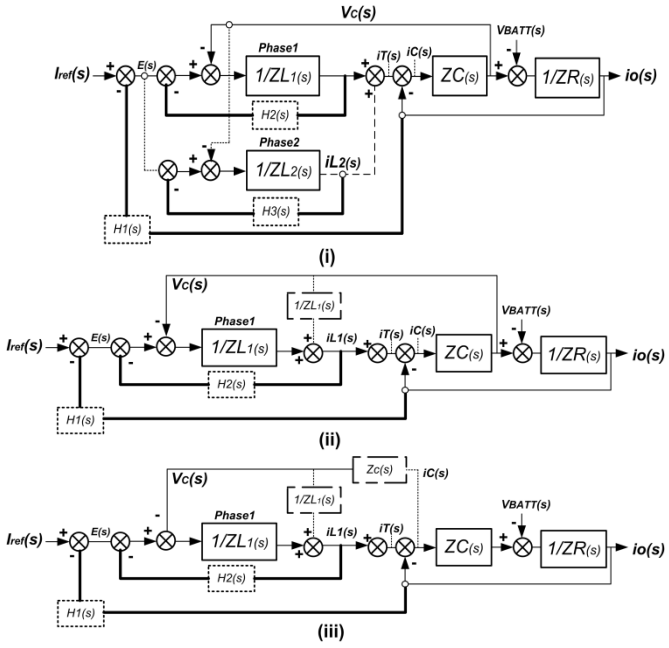

Fig. 1.(i) Conventional CLC current balancing
(ii) Simplified CLC current balancing with capacitor voltage
(iii) Simplified CLC current balancing with total inductor current.

From Eq. (2) and Eq. (3), voltage reference E(s) and capacitor voltage Vc(s) can be seen as control interference to the phase inductor. Increasing the feedback gain H2(S) and H3(s) can significantly reduce the effect of control interference. However, E(s) which depends on the forward loop gain will also reduce. Increasing the gain of the outer-loop is a possible solution, but it increases the oscillations of noise from the output and may lead to unstable operation. Another approach would be introducing an additional feedback to cancel the capacitor voltage effect.

This is shown in Fig. 1(ii), by simply adding another capacitor voltage in front of "Phase 1" block. This arrangement produces new iL1(s) as in Eq. (5),

$$iL1(s) = \frac{Vs(s) - Vc(s)}{ZL1(s)} + \frac{Vc(s)}{ZL1(s)} \quad (5)$$

By further simplifying the Fig. 1(ii) into Fig.1(iii), the total inductor current iT(s) and output current io(s) can also be used as a replacement to the capacitor voltage. Inductor current iL1(s) can now be expressed as in Eq. (6).

$$iL1(s) = \frac{Vs(s) - Vc(s)}{ZL1(s)} + \frac{(iT(s) - io(s))Zc}{ZL1(s)} \quad (6)$$

The implementation of the proposed control scheme is shown in Fig. 2, where Iref represents the desired output current, controller 1 and controller 2 respectively as the outer and inner loop control. Each power switch S1, S2, S3, S4 will have its own switching modulation and interleaved by 90° to ensure optimum ripple cancelation.

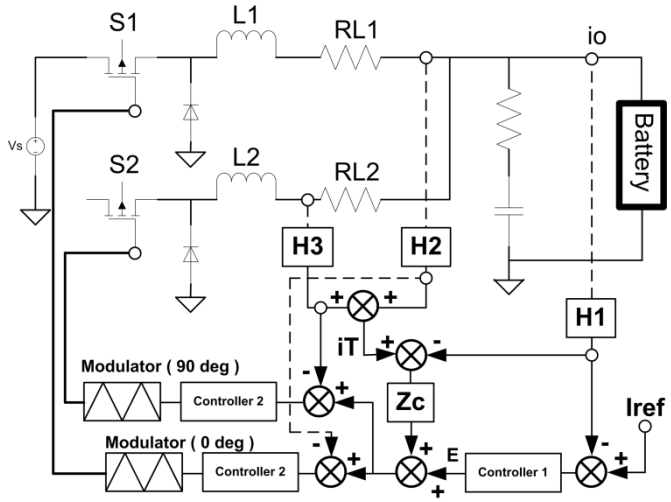

Fig. 2. System configuration of multiphase buck converter.

Since each Nth circuit represent the inner-loop system, an inner-loop transfer function GL1(s) can be obtained as:

$$GL1(s) = \frac{S^2 LCRo + SL + Ro}{1 + SCRo} \tag{7}$$

Assuming unity feedback, Fig. 3(i)(a) shows the step response of Eq. (7) obtained from MATLAB software. The waveform in Fig. 3(i)(a) shows an instantaneous unit step and declined to zero at approximately 3ms. The complete inner-loop response for a four-phase converter can be derived by summing up another three functions in Eq. (7).

This will produce a higher order function and the response time is shown in Fig. 3(i)(b). It is observed that the system response has an initial amplitude value of 0.8 and slower settling time of 16ms. A frequency domain analysis such as bode plot is used to analyze the inner-loop behavior. Fig. 3(ii) shows the bode plot which consists of; open loop, input sensitivity, and output sensitivity. Overall, the system is stable with infinite gain margin and 108° of phase margin. Cross-over frequency at 4.3kHz as shown in Fig. 3(ii) shows that the double switching frequency, approximately 8.6kHz, should be selected to optimize system performance.

For input sensitivity, a maximum attenuation of -25dB implies good disturbance rejection up to its cross-over frequency. However, as it moves above the cross-over frequency, it has saturated to only -1.92dB. This effect can be seen in Fig. 3(i)(b) where the step response reached up to only 0.8. For output sensitivity, it has a DC gain of -0.53dB up to its cross-over frequency which implies constant reference tracking. It has a good noise rejection at a higher frequency with a roll-off rate of 20dB/decade until 16.4kHz as shown in Fig. 3(ii).

The outer-loop transfer function GL2(s) can be derived as in Eq. 8. For simplicity, the core loss RL1-RL4 will be assumed equal.

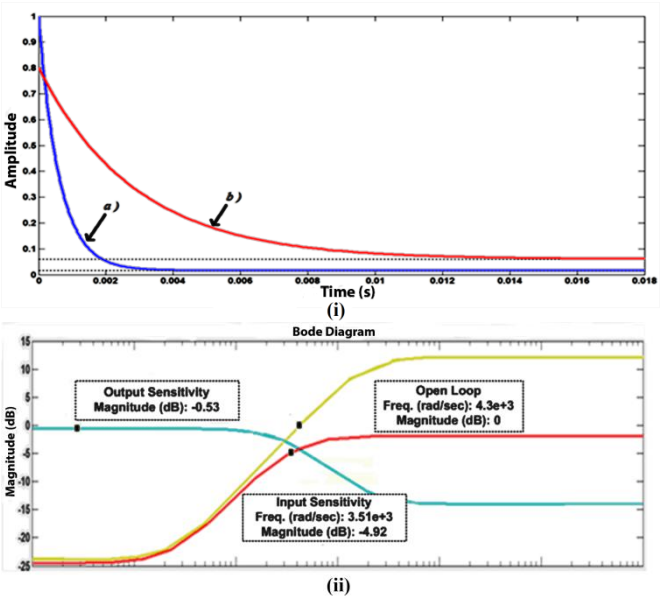

Fig. 3. Step Response and Frequency Domain Analysis: (i) Inner-loop Current Step Response: (a) One-level response (b) Four-level response (ii) Bode diagram of Four-level Inner-loop system

$$GL2(s) = \frac{1/LC}{1 + SCRo} \tag{8}$$

Fig. 4(i) shows the outer-loop response of the system. Although the system has fast settling time of 1.4ms, undesirably it has a very small magnitude of 0.012. Fig. 4(ii) shows the bode plot of an outer-loop system and the output sensitivity. It shows that the open loop system is stable with infinite gain and phase margin. However, any input signal will be attenuated down to -40dB at 4.3kHz and onwards resulting to almost zero output. The input sensitivity has excellent disturbance rejection at -60dB, however, it has low magnitude operation.

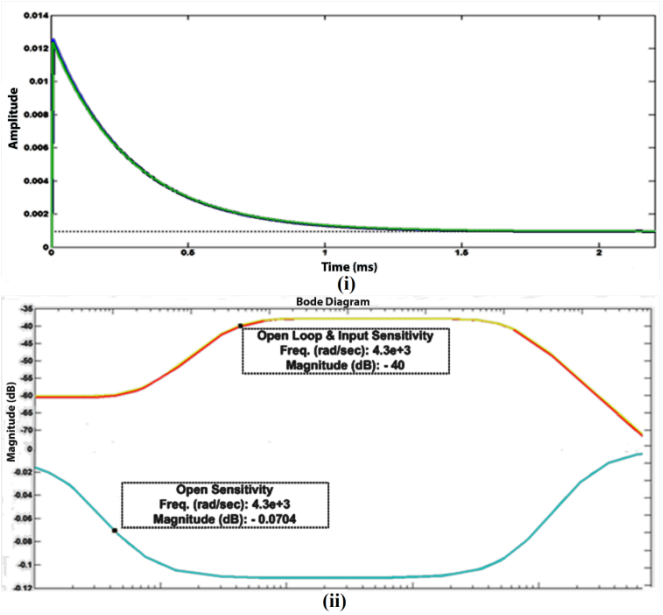

Fig. 4. Step Response and Frequency Domain Analysis: (i)Outer-loop Step Response (ii) Bode diagram of Four-phase Inner-loop system (Open Loop, Input Sensitivity and Output Sensitivity)

From the bode plot analysis, it is concluded that the outer-loop will have a poor control reference since it has very low gain as can be seen in Fig. 4(ii). In order for the proposed system to function properly, the input and output sensitivity of the system must be improved. Increasing the systems gain can improve the step response, however, it will also further deviate the offset value.

After evaluating the bode plot in Fig. 3(ii), the offset deviation is found to be caused by the complex poles and zeros which is located close to 1kHz. Addition, since a switching frequency of 7kHz is proposed, the crossover frequency for the open loop must be adjusted close to 3.5kHz for optimum performance. Table 1, Table 2, and Table 3 shows the parameter used for the proposed converter.

Table 1. Converter specification

Four-phase Multiphase Buck Converter	
Input Voltage (Vs)	10volts
Switching Frequency (Fs)	7kHz
Output Capacitor (C)	5uF
Inductor per Phase (L)	0.6mH
Internal Resistance (Ro)	0.016Ω
Inductor Loss (ohms)	RL1 = 0.1, RL2 = 0.12 RL3 = 0.13, RL4 = 0.14

Table 2. Perimeter for controller 1

Controller 1	
(Gain = 14300 , Real Pole = -3.22)	
Settling Time (millisecond)	4ms
Gain Margin (decible)	78dB
Phase Margin (degrees)	74°

Table 3. Perimeter for controller 2

The Lead Compensator	
Gain	0.1
Real Zero	-1357
Real Pole	-70000
Max Delta Phase (degrees)	74.1°
Frequency (Hertz)	9746 Hz

3. Model Predictive Control (MPC)

Model predictive was first introduced as a computerized controlled algorithm for oil refinery process [12]. It was demonstrated that MPC provides good performance in handling multivariable inputs and nonlinear system. Addition, MPC also possessed robustness as model uncertainty and the restriction does not affect its output performance [12]. As the name implies, MPC relies on model dynamics for prediction, hence a discrete state-space model can be derived as

$$\begin{aligned} X(k+1) &= Ax(k) + Bu(k) \\ Y(k+1) &= Cx(k) + Hu(k) + dk \end{aligned} \tag{9}$$

Where:

$$x(k) = \begin{bmatrix} Vc \\ iL \end{bmatrix} u(k) = \begin{bmatrix} Vs \end{bmatrix} dk = Yc(k) - Yd(k)$$

$$A = \begin{bmatrix} 0 & 1/C \\ -1/L & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & 1/Ro \\ 1/L & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 1/Ro & 0 \end{bmatrix}$$

$$D = \begin{bmatrix} 0 & -1/Ro \end{bmatrix}$$

Within the estimation block, it uses a finite size of horizon (n) to calculate the estimated output Y(k+1)as seen in Eq. (10).

$$\begin{bmatrix} Y(k+1) \\ \vdots \\ Y(k+1+n) \end{bmatrix} = \begin{bmatrix} CA \\ CA^2 \\ \vdots \\ CA^n \end{bmatrix} xk + \begin{bmatrix} CB & \cdots & 0 \\ CAB & CB & 0 \\ \vdots & \vdots & \vdots \\ CA^{n-1}B & CA^{n-2}B & CB \end{bmatrix} .. + \begin{bmatrix} u(k) \\ u(k+1) \\ \vdots \\ u(k+n-1) \end{bmatrix} + \begin{bmatrix} dk \\ \vdots \\ \vdots \\ dk \end{bmatrix} \tag{10}$$

From Eq. (10), the estimation matrix called P, H, L was obtained and forwarded into the prediction block.

$$P = \begin{bmatrix} CA \\ CA^2 \\ \vdots \\ CA^n \end{bmatrix}; H = \begin{bmatrix} CB & \cdots & 0 \\ CAB & CB & 0 \\ \vdots & \vdots & \vdots \\ CA^{n-1}B & CA^{n-2}B & CB \end{bmatrix}; L = \begin{bmatrix} dk \\ \vdots \\ \vdots \\ dk \end{bmatrix}$$

The prediction block uses information such as Yc(k) which represent the converters output, Yd(k) as the model output and model states x(k) to predict (n) numbers of control moves which will guide the system's output to follow the required target references. Concurrently, the optimization

block also helps in calculating the optimum input u(k) using performance index "J" for the MPC online minimization:

$$J = \sum_{k=1}^{n} \left[(Iout - Iref^2) + R(Uerror)^2 \right] \tag{11}$$

Where "R" is the weighting factor and Uerror is the magnitude error between input u(k) and steady state input uss. Solving the output Y(k+1) in Eq. (9) together with Eq. (11) where gradient J = 0 will result:

$$\vec{U(k)} = \left(H^T H + R\right)^{-1} (H^T \left[References - Px(k) - dk \right] ...+ RLuss) \tag{12}$$

Note that uss is the steady state input and R is the control weight. Expanding Eq. (12),

$$u(k) = \left(H^T H + R\right)^{-1} H^T r(k) - \left(H^T H + R\right)^{-1} H^T (P)\, x(k) - \left(H^T H + R\right)^{-1} H^T (L) d(k) + \left(H^T H + R\right)^{-1} (R)(L)(uss)$$

And rearrange into Eq. (13),

$$u(k) = (F_m) r(k) - (K_m)\, x(k) - (M_m) d(k) + (S_m)(uss) \tag{13}$$

Where,

$$F_m = \left(H^T H + R\right)^{-1} H^T$$

$$K_m = \left(H^T H + R\right)^{-1} H^T (P)$$

$$M_m = \left(H^T H + R\right)^{-1} H^T (L)$$

$$S_m = \left(H^T H + R\right)^{-1} (R)(L)$$

From Eq. (13), given that:

$$uss = r(k) / Gss$$

$$-(M_m) d(k) + (S_m) uss = F_m(L) \left[-d(k) + \frac{(R) uss}{H^T} \right]$$

Gss represents the steady state plant. Hence, Eq. (13) can be expanded into Eq. (14).

$$u(k) = F_m \left[P(x(k)) + (r(k)) \frac{Gss + A_m}{Gss} - L(d(k)) \right] \tag{14}$$

It should be noted that,

$$A_m = \frac{L(R)}{H^T} \quad ; \quad B_m = \frac{Gss + A_m}{Gss}$$

From Eq. (14), the control structure based on MPC algorithm is obtained as seen in Fig. 5.

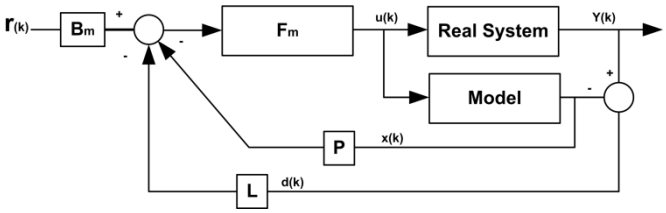

Fig. 5. MPC control block diagram

Since u(k) represents the optimize input with a vector of (n) length, only the first vector is applied by the controller for a certain number of sampling time. At the end of the sampling time, new values of u(k) are recalculated again, this repeated process is called receding horizon. The flow chart for the system can be seen in Fig. 6.

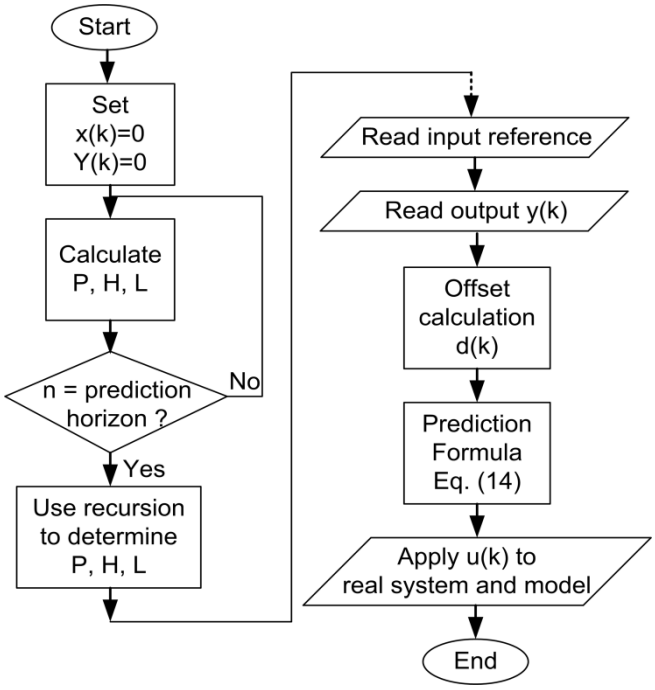

Fig. 6. Flow chart of MPC

4. Simulation Results

Using sampling time of 0.1ms and the parameters shown in Table 1, a discrete model was obtained as shown in Eq. (15). The performance of the multiphase buck converter is

$$Az = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \quad ; \quad Bz = \begin{bmatrix} 0.02 & 0 \\ 0 & 0 \end{bmatrix}$$

$$Cz = \begin{bmatrix} 0 & 0.75e-3 \end{bmatrix} \; ; \; Dz = \begin{bmatrix} 62.5 & -62.5 \end{bmatrix} \tag{15}$$

demonstrated under MATLAB/Simulink software. The system is tested under three operating conditions; step load changes k1, step current changes k2, and step input changes k3. Fig. 7 and Fig. 8 show the waveforms for input voltage, output current, output voltage and inductor current for both conventional CLC current balancing and the proposed system.

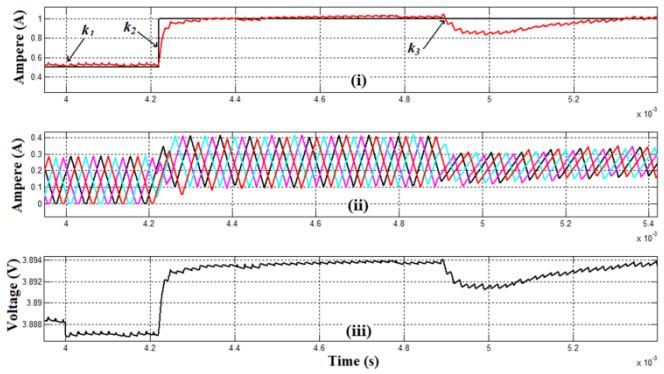

Fig. 7. Proposed system during step changes: (i) Output current (ii) Inductor current L1, L2, L3, L4 (iii) Output voltage

Initially, both control schemes are operating at a reference of 0.5(A/s) output with balanced inductor current in all phases. During a step k1, both output current, and inductor current remains constant while output voltage drops instantly from 3.888(V/s) to 3.887(V/s). During k2, both control schemes require 0.1ms of settling time when the reference current increases from 0.5(A/s) to 1(A/s). It is observed that both the inductor currents remain balanced. At k3 with input disturbance from 10(V/s) to 7(V/s), both output current and voltage requires 0.4ms to recover.

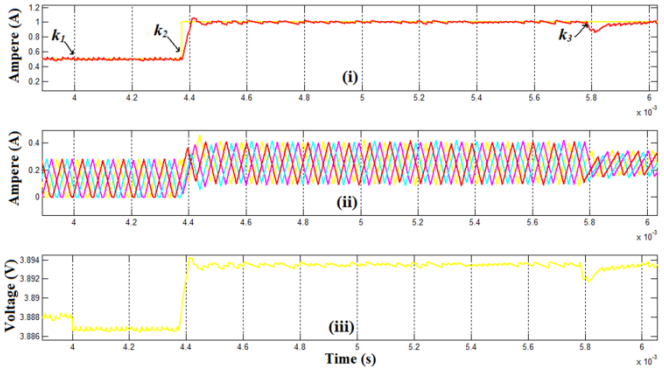

Fig. 8. Linear response of four-level multiphase buck converter during step changes: (i) Output Current (ii) Inductor current L1, L2, L3, L4 (iii) Output Voltage

Figure 7 and 8 shows that inductor current of all phases remains balanced. Table 4 shows the performance comparison between proposed system and conventional CLC current balancing.

Table 4. Comparison of different control schemes

	Proposed Control	**Conventional CLC**
	Predicted Horizon : 10 Control Horizon : 3 Weighing Factor : 50	Table 2 parameters + Lead Compensator
Step Current	0.1ms	0.1ms
Input Disturbance	0.4ms	0.21ms
ΔV /ΔI (ripple)	4.8% ; 0.01%	8% ; 0.05%

5. Experimental Results

Fig. 9 shows the developed laboratory prototype for a four-phase buck converter usingTMS320F28335 as the controller. The parameter used are as follows; input voltage (Vs) = 10V, inductor (L) = 630uH, filter capacitor (C)=5.6uF, inductor loss (RL) = 0.1/0.15Ω, MOSFET switch SI4124DY, power diode ES2AA-13-F, current sensor ZXCT1009 and a lithium-ion battery SV-HK-10E. The measurement data are collected using Tektronix TDS-2024C oscilloscope.

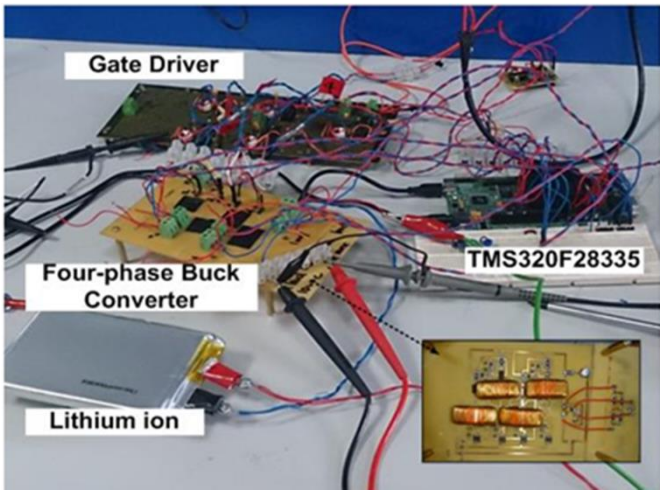

Fig. 9. Hardware setup of four-level multiphase buck converter.

Fig. 10 and Fig. 11 shows the waveforms of an input voltage, output current, output voltage and inductor current for both proposed system and conventional CLC current balancing. Initially, both controllers are operating at a reference of 0.3A output. From Fig. 10 and 11, it is observed that inductor current iL4 for conventional CLC current balancing control has a higher magnitude than the others (iL1, iL2, iL3) for once in every few cycles. While inductor current of each phase in the proposed system remains balanced. At m1, both systems require 300us of settling time to reach 0.6A and the inductor current of each phase for both systems are still balanced. The output current is reduced to 0.5A at m2 and the proposed system shows that the current of all phases are more stable than the conventional CLC current balancing control. At m3 when the input voltage drops from 10V to 8V, Fig. 11 for the proposed system shows that the current of all phases are more stable and respond faster than the conventional CLC current balancing control.

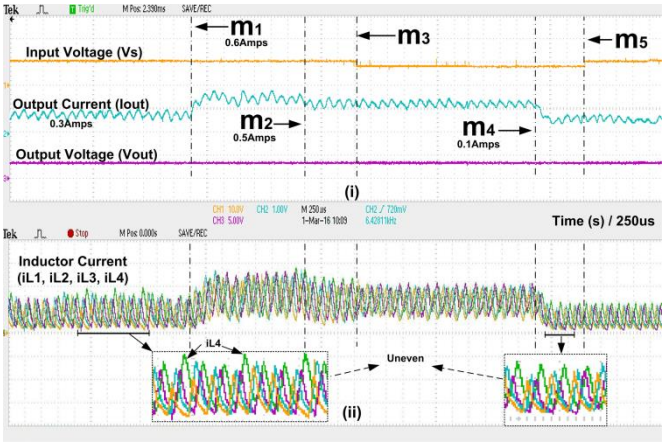

Fig. 10. Experimental results for the conventional CLC current balancing control.

At m4, the output current reference is changed to 0.1A with a settling time of 250us for both systems. Again, at this point, it is observed that inductor iL4 from the conventional CLC current balancing control has the highest magnitude. While inductor current of each phase in the proposed system remains balanced. At m5, the converter's nominal voltage is restored to 10V subsequently both controllers still able to maintain balance current sharing in the inductors. However, the proposed system inductor currents are more stable.

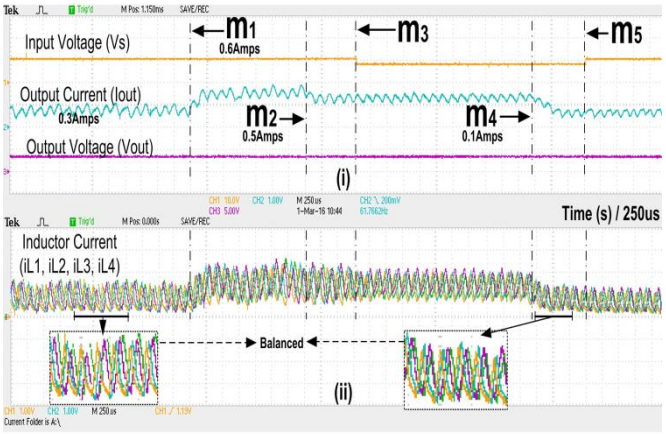

Fig. 11. Experimental results for the proposed system.

6. Conclusion

This paper has presented a control scheme to mitigate unbalanced phase current in a four-phase buck converter. The investigation is carried out under two types of control strategies; conventional CLC current balancing control and the proposed system. From the analysis of inner and outer loop using conventional CLC current balancing control, it is concluded that overall performance and suitable compensators must be added to improve the gain and response of the system.

As the complexity increases, balanced current can be achieved at the expense of complex design and limited bandwidth operation. The simulation is validated with the experimental setup, and, it is observed that the proposed system is effective in handling unbalanced phase current in; variable load current, variable input source, and, uneven resistive value between each inductor.

In terms of controller design and hardware implementation, the used of MPC is more straightforward and the algorithm is easy to program. Designing with the conventional CLC requires a fully understanding of the required system behavior and detailed analysis is required such as frequency domain analysis.

Acknowledgements

This research was supported by Fundamental Research Grant (FRGS) and, Ministry of Higher Education, Malaysia (Project code: 20140120FRGS).

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