# An improved Resonant Fault Current Limiter for Distribution System under Transient Conditions

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**Abstract-** In this paper a modified fault current limiter has been designed for limiting the short circuit current under transient condition. In order the provide security for the distribution network a properly designed fault current limiter is needed. In the present approach a resistor is being connected in series with capacitor and this structure is later connected with inductor which maintains the fault current at prefault level. With such type of topology the voltage at point of common coupling does not experience any sag during the fault occurrence. For limiting the fault current and operate the system under particular voltage levels many topologies are implemented, some of them used reactors, superconducting fault current limiter, solid state FCl, resonance type are usually implemented. The main advantage of this type of fault current limiter is that it doesn't require any superconducting inductor because of its high cost. The performance of this resonance fault current limiter is briefly discussed and simulations are done in MATLAB/SIMULINK.

**Keywords** Fault current limiter, line reactor, voltage sag, Power quality

## 1. Introduction

One of the main objective of the power system is to achieve high reliability [1,36]. Due to continuously increasing in the power demand and high penetration of the renewable energy resources at the distribution level there is also high magnitude of fault current level [37]. The occurrence of fault and its troubleshooting is a great challenge [3,38] for achieving secure operation of various complex systems. We can define power quality as the ability of an power system to deliver the power to the consumer loads meeting the desired specifications of the load. Now a days due to excessive growth of power system network there arises few problems in maintaining quality in the power supply [1]. One of the power quality problems is the voltage sag and this occurs due to sensitive loads [2,43]. There are many reasons for voltage sag, among them short circuit is the major cause for voltage sag. When voltage decreases, current reaches to maximum value which is not safe for operation of electrical components at the consumer end [3],[4].

When a fault occurs at any location in the present power system scenario the fault current may reach to or sometimes may even exceed the maximum limit of the protective devices mostly circuit breakers [1,36,40].The fault current can be minimized by superconducting fault current limiter [19] which is having the capability to change the impedance under normal and fault conditions. As the availability and cost of superconducting material is not impressive so we are implementing a non-superconducting material which is having a low power loss compared to power loss in the feeder. There are various superconducting fault current

limiters (SFCL) [30-32] presently implemented and are on live at many locations.one such SFCL has been commissioned by using a cryogenic system is presented in[36] for a 220KV/300 MVA. This offers a low impedance while it is under normal operating condition and introduces a large impedance when a short circuit occurs [2,44-47].Thus FCL are not only used to restrict or control the short circuit current but they are also used for improving the power quality, increasing the reliability of power supply and power transfer [8-10,36,47].There are many other FCL like solid state FCL, resonance type SFCl. In [39] proposed a resistive type SFCL by utilizing the magnesium diboride,it offers the advantage of low weight and compact structure. Due to continuous integration of renewable energy sources [45-49] there is an need to monitor and control the ever rising faults levels in the distribution system. Sometimes the fault currents are present in the electrical network that may even exceed the permissible value of the circuit breakers[40,41]. Sudden variations in the magnitude of fault current will result in coordination problems in the overcurrent relays[42,43,49]. Here we are implementing a resonant type FCL, resonance in the system occurs only when an L and C are connected either in parallel or series. Suppose if the L and C are connected in series then it will oppose the sudden rise in the fault current on the occurrence of a fault. The drawback of this type of construction is that, if the fault is persisting for more time then it will not limit the fault current even after certain duration of time interval. In the existing topology of resonant type FCL we have used a circuit in such a way that resonance condition arises among L and C[1]. But this also results in large oscillations and can damage the system equipment in large magnitude [23,35]. In the proposed topology a capacitor is placed in series with a resistor and it helps to vary the load impedance during fault. This will fix the fault current up to the prefault condition.

The main advantage if this king of resonant type FCL is that it is not being implemented with the superconductor. So it is simple to manufacture and reduce the cost also. The oscillations are also avoided by using a resonant circuit which consists of resistor and capacitor in series manner.

## 2. Principle of Operation

**Existed model:**

The circuit shown in Fig.1. consisting of a diode bridge rectifier and a reactor ($L_{dc}$) in series with a resistor $R_{dc}$. It is connected in parallel with a diode and the complete pair is connected to a IGBT. Here the diode D5 acts as freewheeling diode. The bridge rectifier is shunted with a series combination of $L_{sh}$ and $R_{sh}$ i.e. ($R_{sh}$+jw$L_{sh}$). Here $L_{dc}$ is used to prevent high magnitude of di/dt when the fault occurs. As this system is producing more power losses we have modified the system in such a way that the power losses are reduced and line current oscillation also been overcome by connecting a resistor in series with capacitor in parallel with $L_{sh}$.

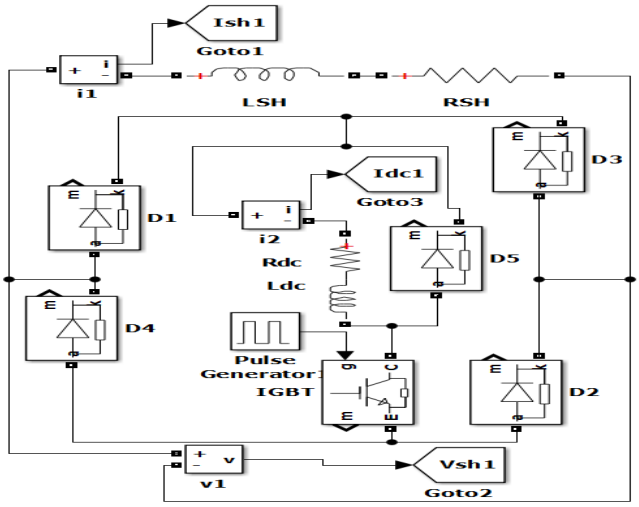


**Fig.1.** Diode bridge rectifier with $L_{dc}$ for fault current prevention

**Modified model:**

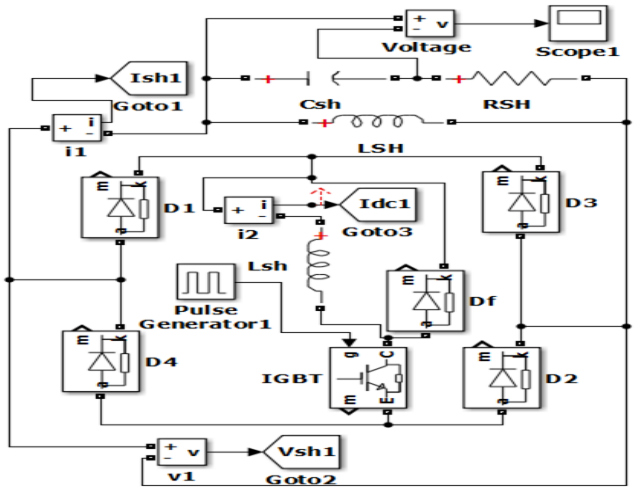


**Fig.2**.Modified fault current limiter

Here we have eliminated $R_{dc}$ and connected a capacitor and a resistor in parallel with $L_{sh}$ this is the circuit topology for a single phase circuit and similarly we can connect for three phase distribution system also. The circuit is mainly classified as follows:

Section1: It is clear from Fig.2. that it consists of a rectifier bridge of 4 diodes D1-D4,a reactor $L_{sh}$, a self-turn off switch(IGBT) placed and a freewheeling diode($D_f$) placed in parallel with $L_{sh}$.

Section2: This is the main part of the resonant FCL i.e. it comprises of a parallel LC resonant circuit. The resonance frequency is same as that of the fundamental frequency and $R_{sh}$ is connected in series with the $C_{sh}$ and it is in parallel with the inductor $L_{sh}$.

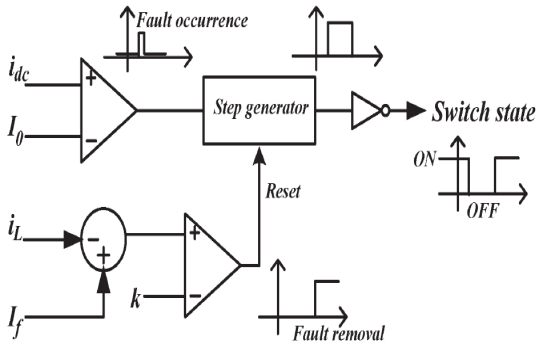


**Fig.3.**Control circuit for the FCL where the switching action takes place

## 3. Operation of Fcl:

Whenever fault occurs in the system, the proposed FCL operates instantaneously and diverts the current due to the fault path to the resonant path. The main advantage of this proposed circuit consisting of a diode bridge rectifier instead of two anti-parallel switches [22] is that

a. It uses only one semiconductor switch that is being operated on DC side, whereas the two switches will operate on AC side so during the normal operation there is no need of switching the devices.
b. Here the semiconductor is placed in series with reactor is having two advantages
   i. It looks like a snubber circuit for a semiconductor switch.
   ii. Whenever a fault occur it acts as current limiting device(inductor opposes sudden change in the current).

The voltage across the line reactor is negligible when compared to feeder voltage so the voltage drop is not considered in this aspect. Whenever a fault occurs in any system the current and voltage are expected to reach dangerous values. So we can use snubber circuits which are rated at 24 KA and 4KV. The snubber circuits are used to limit high current and voltages either [27].

Under normal working conditions the power loss in the FCL can be calculated as

$$P_{loss} = P_R + P_D + P_{SW} = I_{dc}^2 R_{dc} + 4V_{DF} I_{ave} + V_{SWF} I_{dc} \quad (1)$$

Here
$I_{dc}$= DC Current
$R_{dc}$= Reactor resistance
$V_{DF}$= voltage drop across the diode
$V_{SWF}$=Semiconductor switch voltage drop
$I_{ave}$= average current of the diode

The total power loss is negotiable when compared to feeder transmitted power.The operation of fault current limiter is as shown in Fig.3.When the system is under normal working condition the switch is under ON state and the $L_{dc}$ is being charged to peak value and it behaves as dead short circuited. But when the fault occurs the DC current reaches to maximum allowable limit and cross the $I_0$ value and thereby it turns off the semiconductor.

During this condition the freewheeling diode will provide a path for continuous conduction for discharging the reactor. Now the fault current creates large impedance into the circuit and suppresses the fault current. Till the fault is being cleared the circuit will resonate with large magnitude [23,34] of line current. Sometimes these large magnitudes of line current may damage the system equipment. This situation is avoided by placing a series resistor and a capacitor so that the current transients will damp out quickly. Though the fault has been removed the switch is still under turnoff condition but the load is in series with the parallel part. So because of this reason only the line current will be reduced instantaneously.

The fault current is calculated as

$$I_f = \frac{V_{pcc}}{Z_{eq}} \quad (2)$$

the semiconductor switch will comes to turn on state of $i_c - i_f > k$ and this gives the sign that the power system is under normal state
The value of K is given by

$$K = \frac{V_{pcc}}{Z_{eq}} - \frac{V_{pcc}}{Z_{eq}+Z_{lmin}} \quad (3)$$

Here $Z_{lmin}$ is the min impedance of the load.

As the inductor is being bypassed under normal working condition by a bridge topology, so it has low losses at the

resonant condition. We need to select an appropriate value for the resonant circuit without affecting the power system under fault. Therefore the system is not affected by any voltage sag.

## 4. System Analysis With Various Modes Of Operation

As shown in the Fig.4. it consists of a voltage source, a step up transformer, a CB and the load connected through line impedance.

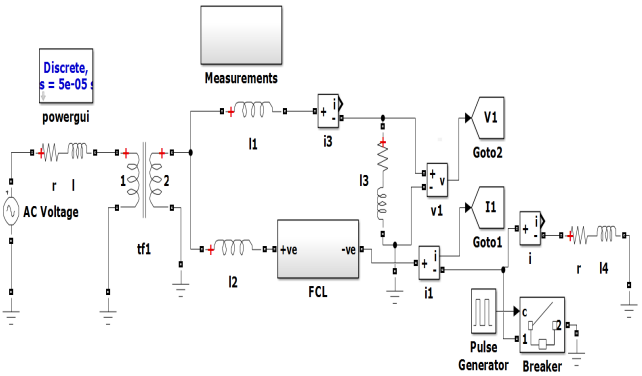


**Fig.4.**Simulation model of fault current limiter implemented for one of the phase of the transmission line.

The important part of this system is the bridge and the FCL. If there is any chance of permanent failure due to short circuit the circuit breakers are rated for meeting such situations also.

In this aspect there are two modes of operation

Mode1: When the power system is under normal operating condition the line current($i_L$) is expressed as

$$i_L(wt) = \left(\frac{V_s}{\sqrt{R^2+w^2L^2}}\right)\left[\left(\frac{L_w}{\sqrt{R^2+w^2L^2}}\right)e^{-\left(\frac{R}{wL}\right)wt} + \sin(wt-\varphi)\right] \quad (4)$$

Here $\varphi=\arctan\left(\frac{wL}{R}\right)$

Mode2: When a fault occurs, the $L_{dc}$ opposes the current and limits the rate of fault current to increase instantaneously. Till the reactor reaches to its maximum line current value the semiconductor switch will not operate.

At $t_{sw}$ the bridge is switched off and the resonant circuit comes into operation and maintains the fault current at predefined value or the safe value.

The predefined current $I_o$ is given by

$$I_o = i_L\ (t= t_{sw}\ )$$

$$\left(\frac{d_{iL}}{dt}\right)(t = t_{SW}) = \frac{V_s \sin(wt_{SW}) - I_o(R_s+R_{sh})}{L_s} \quad (5)$$

$$\left(\frac{d^2 i_L}{dt^2}\right)(t = t_{SW}) = V_s\omega\cos(\omega t_{SW}) + I_o\left(\frac{R_{sh}^2}{L_{sh}} - \frac{1}{C_{sh}}\right) - \left(\frac{V_s \sin(\omega t_{SW}) - I_o(R_s+R_{sh})}{L_s}\right)(R_{sh}+R_s) \quad (6)$$

Now solving the above equation we get

$$L_s L_{sh} C_{sh}\left(\frac{d_{i_L}^3}{dt^3}\right) + (R_s L_{sh} C_{sh} + L_s R_{sh} + R_{sh} L_{sh} C_{sh})\left(\frac{d_{i_L}^2}{dt^2}\right) + (L_s + R_{sh} C_{sh} R_s + L_{sh})\left(\frac{d_{iL}}{dt}\right) + R_s i_L = (V_s - L_{sh} C_{sh}\omega^2)\sin(wt) + R_{sh} C_{sh} V_s w\cos(wt) \quad (7)$$

When the transient are damped out i.e. transient are minimized the fault current equation can be expressed by

$$i_L = A\cos(\omega t) + B\sin(\omega t) \quad (8)$$

Now by adjusting or varying the values of $L_{sh}$,$C_{sh}$ and $R_{sh}$ the line currents are under prescribed limits during the fault condition. Even though the fault occurs PCC voltage doesn't have any effect.

## 5. System Design

It is well known fact that the inductor never allows sudden change in current due to its magnetizing property. In the same manner here $L_{dc}$ is used for blocking the fast increasing fault current and makes the semiconductor to turn off in a safe condition. The values of $L_{dc}$ can be selected on observing the semiconductor current characteristics/ In any electrical circuit maximum power can be transferred if the load impedance is equal to system impedance. Likewise for a resonant circuit also the resonant part equivalent impedance must be equal to the load impedance.

The equivalent impedance of the resonance part is given by

$$Z_{eq} = \left(R_{sh} - {}^{j}/_{\omega C_{sh}}\right) \| \ j\omega L_{sh} = {}^{L_{sh}}/_{C_{sh}R_{sh}} + j\omega L_{sh} \quad (9)$$

The resistor values must be chosen in such a way that the load resistance will be equal to $L_{sh}/C_{sh}R_{sh}$. But it is practically not possible to make it as equal due to variation of load on the distribution side.

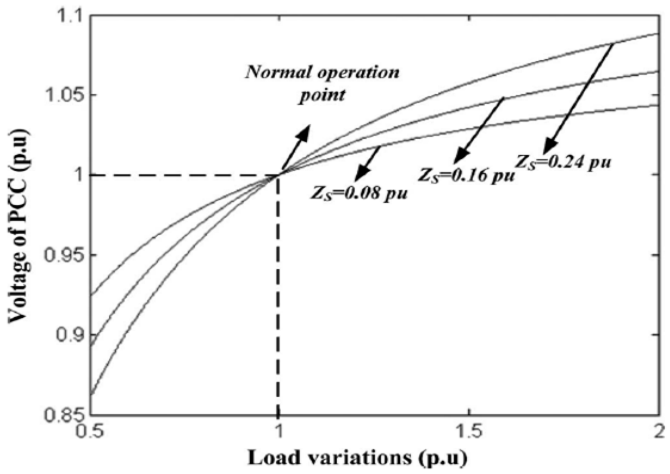


**Fig.5.**The PCC voltage when the resonance impedance is not equal to the protected feeder impedance.

In the Fig.5. the horizontal axis represents the load impedance in p.u, the dashed lines represent the ideal case. It can be stated that for a wide variation of load the voltage at the PCC change in small permissible value i.e. acceptable values particularly for low values of $Z_s$

If we consider the heating effect that arises in the resistance present in the resonant part, then it is possible for changing $L_{sg}$, $C_{sh}$, $R_{sh}$ values and reduces the real part of the equivalent impedance equation.

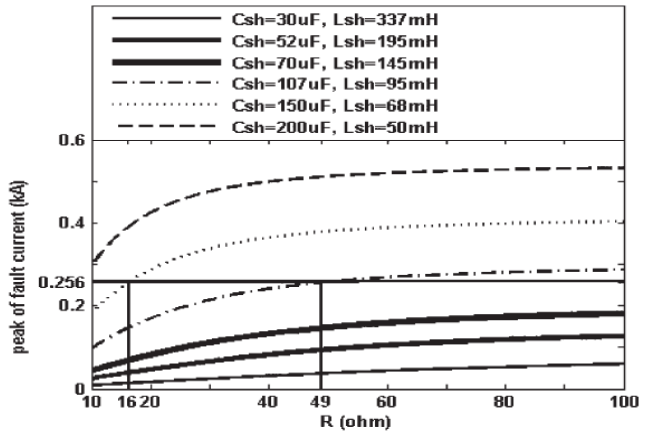


**Fig.6.**Change in the fault current with variation in the resistance.

The variation of fault current with $R_{sh}$ is shown in Fig.6.To have a better transient response $R_{sh}$ is chosen to be low value. We obtain the values of $C_{sh}$ from [33].Now the $L_{sh}$ values is determined taking into consideration the resonance between L and C at power frequency.

Let us consider one example

i.If the feeder average current is 256A then the desired fault current can be achieved in two different ways

a. Taking $C_{sh}$=150uF,$L_{sh}$=68mH,$R_{sh}$=16ohm

b.$C_{sh}$=102uF,$L_{sh}$=95mH,$R_{sh}$=46ohm

In the above cases the values of load impedance $Z_{eq}$ is equal but the real part of case2<case1.Therefore the heat generated in the $R_{sh}$ is reduced at the instant of fault occurrence.

## 6. Simulation Results

Here we are analyzing the system on considering the Fig.3. topology during the fault. A list of parameters for simulation is shown in table1. We are introducing a fault in between the time period of 0.1s to 0.2sec. During the fault condition the line currents are studied for three different cases shown in Fig.7 to Fig.9.

It is clear from the Fig.7. that the fault current is reaching dangerous value if we are not using the FCL it is also asymmetrical due to unbalance condition occurring in the system, If we observe the similar system without using $R_{sh}$, the transient oscillations are present as shown in Fig.8 .Now after damping all the transients, the line current is made near to zero.

**Table 1**
Simulation System Parameters

| | | |
|---|---|---|
| **Source Side Data** | Voltage Source | 20 KV |
| | Step down Transformer | 20KV/6.6KV |
| | Transformer Rating | 10 MVA |
| **FCL Data** | Dc Side | $L_{dc}$= 0.01H |
| | Resonance Part | $L_{sh}$= 0.068H,$R_{sh}$=16Ω,$C_{sh}$=150uF |
| **Load Side Data** | $Z_{line}$=0.5 Ω,and $Z_{load}$=15+iω0.1 Ω | |

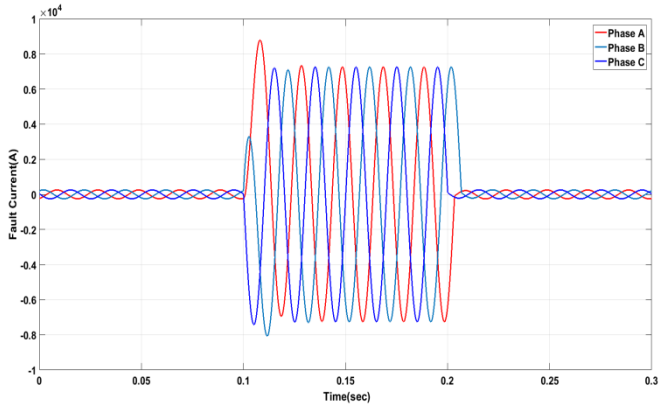


**Fig.7.** Fault Current $i_L$ Without FCL.

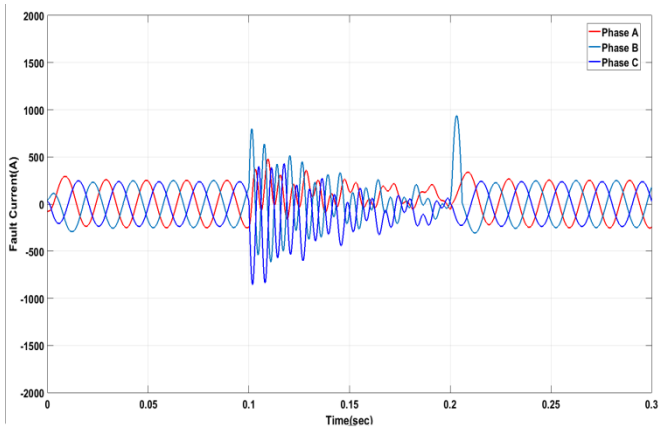


**Fig.8.** Fault Current $i_L$ Without $R_{sh}$ in the resonance type FCL.

When we introduce a FCL into the system the line current during the fault reaches to $I_o$ which is the minimum fault current and under such condition the line current is maintained at nominal value by turning off the semiconductor switch. Later when the fault is being removed the semiconductor switch is turned on and therefore the line current will comes to its nominal value after having negligible distortion as shown in Fig.9.

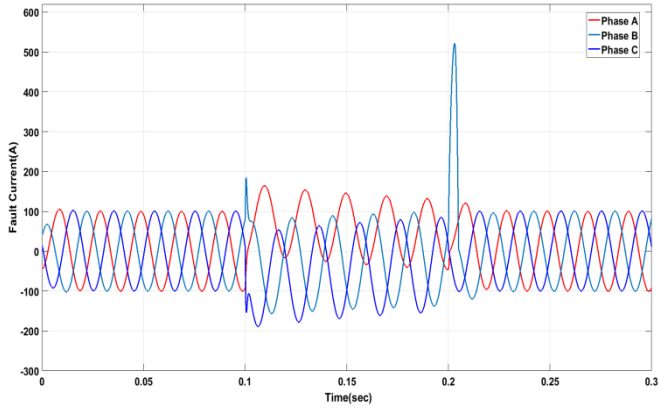


**Fig.9.** Fault Current $i_L$ With the proposed FCL.

From Fig.10. We can understand that the dc reactor start charging till the semiconductor turns off. When the reactor is fully charged the semiconductor switch is turned off and the freewheeling diode operated discharging the $L_{dc}$.

The resonant current flowing through the shunt part $I_{sh}(t)$ for A phase and this is equal to the line current when the semiconductor switch is being operated.

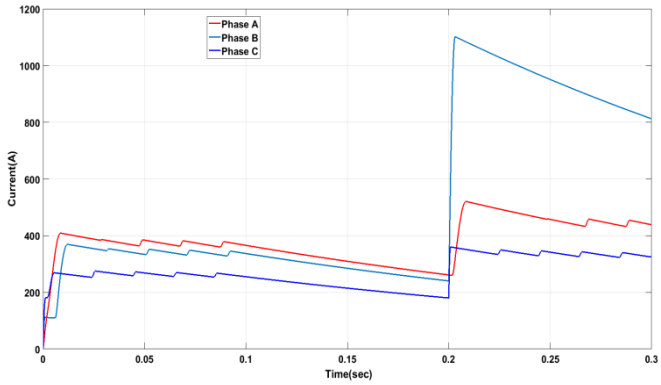


**Fig.10.** Dc reactor current for all the three phases.

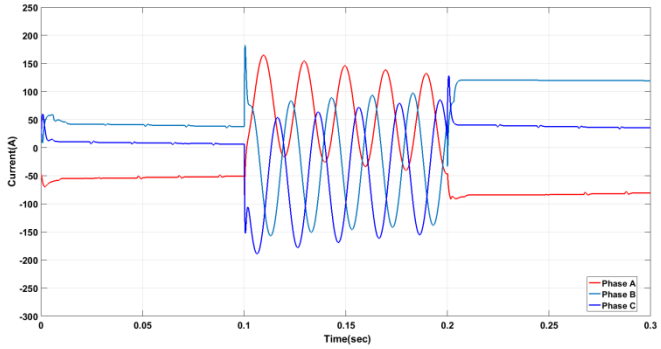


**Fig.11.**Resonant part during fault for all the three phases.

This is shown in Fig.11.It has been observed that the distorted waveform on the PCC voltage is due to the presence of resonance current. The voltage across the capacitor in the phase A is shown in fig 12.

It has been stated that for all semiconductor devices the turn on will be based on the peak value of the fault current and this can be also be taken as the rating of $L_{dc}$ similarly the turn off depends on the voltage at the instant of fault occurrence.

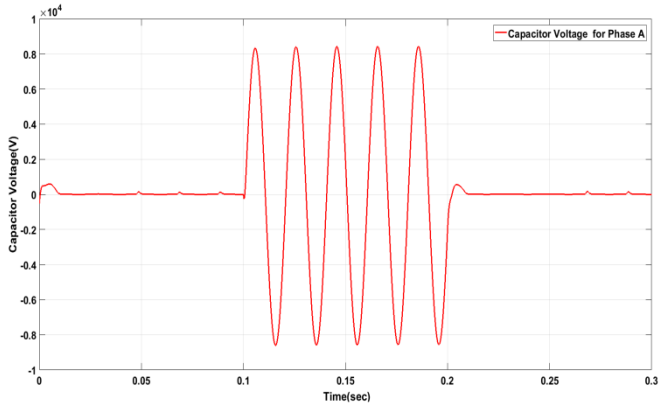


**Fig.12.**Capacitor voltage $V_c(t)$ for Phase A.

## 7. Conclusion

So, by implementing a parallel resonance fault current limiter the magnitude of fault current has been maintained at 100A to 180A and coming to steady state after 0.2sec.as compared to previous value of 550A without this topology. The resonance part $i_{sh}$ during the fault also minimized to 150A. The system has been studied with and without implementing resonance fault current limiter. Some of the fault current limiters is having few drawbacks that was previously discussed and this topology is having the ability to improve the power quality also. This also maintains considerable amount of PCC voltage during the fault. So, during the transient fault condition there is no need to open the circuit breaker and therefore the $R_{sh}$ will be present in the system to dampout the oscillations. It also maintains the fault current constantly which is not achieved with series resonant type fault current limiter.

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