# Performance Evaluation of SEPIC Based Single-Phase Seven-Level Inverter for Renewable Applications

Arunprasath R*, Vijayakumar D**‡, Rathinakumar M*, Meikandasivam S**, Kirubakaran A***

* Department of Electrical Engineering, SCSVMV University, Enathur, Kanchipuram-631561, India

** School of Electrical Engineering, VIT University, Vellore-632014, India

*** Department of Electrical Engineering, NIT Warangal, Warangal-506004, India

(prasatheee2003@gmail.com, vijayakumar.d@vit.ac.in, meikandasivam.s@vit.ac.in, rathinamari@rediffmail.com, kiruba81@nitw.ac.in)

‡ Corresponding Author; Vijayakumar D, School of Electrical Engineering, VIT University, Tel: +90 9952068961,vijayakumar.d@vit.ac.in

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**Abstract-** Contemporary research in multilevel inverters (MLIs) is becoming famous for low power renewable applications. In this paper, therefore, a new configuration of SEPIC based single-phase seven-level inverter is presented with the advantages of lower parts count, size, and reduced cost. The front-end sepic inverter is used to boost the input voltage to the desired voltage and cascaded with a 1:2 multi-winding high-frequency transformer to generate $V_{dc}$ and $2V_{dc}$ which is fed to the asymmetrical six switch multilevel inverter. The simulation work is carried out in Matlab/Simulink environment, and a laboratory prototype model is developed to validate the concept. The control pulses for the SEPIC inverter is built using TMS3202812 DSP in real time workshop(RTW), and the switching pulses for MLI are generated using a Spartan-6 FPGA Processor. The performance of the proposed topology evolved for the step change in input voltages, and the different loading conditions. A detailed comparison of various seven-level inverter topologies is also conducted.

**Keywords** SEPIC inverter, Multilevel inverter, Digital signal processor (DSP), Field programmable gate array(FPGA), total harmonic distortion(THD).

## 1. Introduction

The concept of the multilevel inverter (MLI) is invented long year ago with the traditional three popular topologies of (i) Neutral point clamped inverter (NPC-MLIs), (ii) Flying capacitor inverters (FC-MLIs), and Cascaded H-Bridge inverters (CHB-MLIs). It synthesis the multilevel output voltage waveform with the advantages of reduced voltage stress across the semiconductor devices and lower total harmonic distortion for the increase in levels [1]. All these topologies are suitable for medium/high voltage industrial applications. However, their output levels are limited due to the difficulties in balancing of dc-link capacitor voltages, increased device counts, driver circuits, control complexity and need of more dc sources. Extending the applications of MLI for low power applications will enhance the quality of output waveforms, reduction in the size of the filter components and improvement in overall efficiency of the system. Therefore, recent research on MLIs with reduced device counts is becoming popular for low power/voltage rating renewable applications.

Several MLIs had reported in the recent literature with their own merits and demerits in terms of device counts, driver circuits, passive components, and voltage blocking capacity [2-6]. The staircase multilevel output voltage waveform is achieved by using many dc sources or combination of capacitors in series/parallel conversion [7-9]. The multilevel output voltage levels can be made either by symmetric or asymmetric configuration. The source consists of photovoltaic, fuel cell or battery energy storage systems are connected with few cells and always operated with lower dc output. Employment of multi dc source with independent maximum power point tracker (MPPT) control can be a

better solution for photovoltaic based applications [10]. However, increased number source and components will leads to increase in cost, size and volume for low power applications. For that, a seven-level inverter with reduced components and a single dc source is proposed in [11]. But this configuration is more suitable for the resistive load, and the control scheme for balancing the capacitor voltage becomes more complicated for an increase in levels. The above-said configurations are non-isolated, and the elimination of leakage current problems demands additional filter circuit. The use of isolated topologies avoids the need for other EMI filters to address the leakage current problems in the photovoltaic system [12].

The use of conventional dc-dc boost converter with the single switch cannot provide higher voltage gain and also operates at a higher duty cycle to increase the output voltage. Many novel techniques of voltage doubler circuit and interleaved concepts are adopted to improve the voltage gain [13-14]. Whereas, these configurations increase the components and affect the efficiency of the system. For that, a SEPIC based converter is proposed which can perform both buck and boost operations [15]. Owing to the advantages of SEPIC converter, its input inductor reduces the input current ripple and also the limitations of the gain can be resolved with the use of a high-frequency transformer.

Therefore, this paper presents a new configuration of SEPIC based seven-level inverter with the significant features of reduced device counts, driver circuits, modular structure, improved power quality and higher efficiency. The performance of the proposed model tested in Matlab software. A prototype model is developed to validate the concept. Closed loop control scheme is implemented using TMS320F2812 digital signal processor (DSP) in real time workshop (RTW). Whereas, the control pulses for seven-level inverter is built using Xilinx blocks with SPARTAN 6 FPGA boards. Moreover, a comparison of various seven-level configurations is presented to show the significance of the proposed topology.

## 2. Proposed Configuration

Fig. 1 shows the proposed SEPIC based seven-level inverter configuration. It consists of a front-end SEPIC converter cascaded with six-switch seven-level inverter through a high-frequency multi-winding transformer. The proposed SEPIC converter boosts the change in input voltage to desired $V_{dc}$ value, and the multi-winding secondary of HF transformer is used to produce $V_{dc}$ and $2V_{dc}$ voltage which is fed to the asymmetrical multilevel inverter to generate seven-levels.

The appropriate gating signals are generated using DSP and FPGA processors. The detailed descriptions of the configuration are as follows;

### *2.1. SEPIC Converter*

The single-ended primary inductor converter (SEPIC) is capable of supplying the desired output voltage either greater than or less than or equal to the input voltage by controlling the duty cycle ($d$) of the converter. These converters require two-inductors to regulate the output. Fortunately, one of the inductors is act as primary of the high-frequency transformer which results a reduction in size and volume of the converter is one of the advantages of the proposed configurations. Fig. 2 depicts the closed-loop control of the SEPIC converter. The varying input voltage ($V_{sensed}$) compared with the set reference voltage ($V_{ref}$) and the error passed through PI controller which generates the required duty cycle and compared with the carrier signal to build the firing pulses for the control of Mosfet of the SEPIC converter.

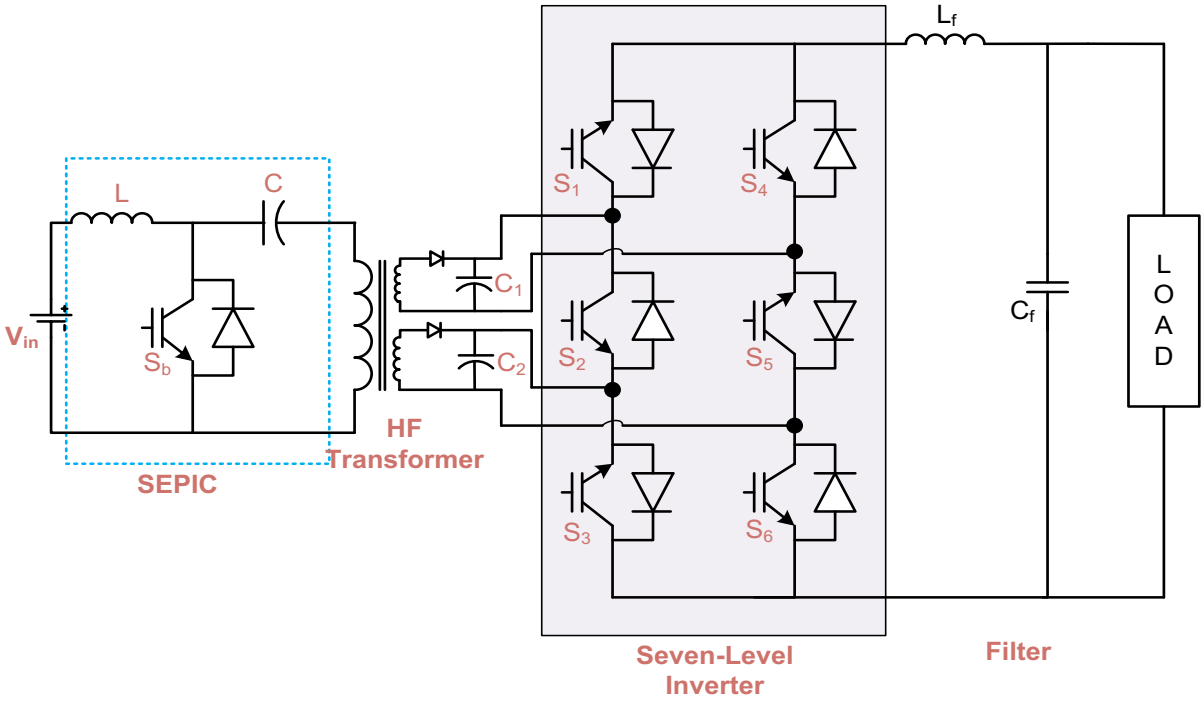



**Fig. 1.** Proposed SEPIC based single phase seven-level inverter.

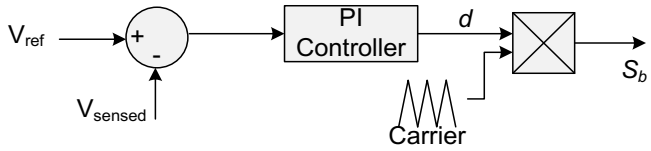



**Fig. 2.** Closed loop controller for SEPIC converter.

The selection of inductor and capacitor also decides the response of the converter and also cost of the system. The larger size of $L$ & $C$ is more expensive and more internal resistance. So proper selection of ripple values best values of $L$ & $C$ can be chosen. Here the input inductor and capacitor can be selected using the following expression [15];

$$\frac{V_o}{V_{in}} = \frac{D}{(1-D)} \tag{1}$$

$$L = \frac{DV_{in}}{f_s \Delta I_L} \tag{2}$$

$$C = \frac{DV_{dc}}{Rf_s \Delta V_C} \tag{3}$$

*2.2. Seven-Level Inverter*

This modified configuration constructed by using the six-switch seven-level inverter presented in [16]. The benefit of the six-switch converter is not well addressed in any literature with front end converter and single DC source. Most of the research focuses on the use of more number of dc sources only. The level generation can be addressed in three different modes of operation.

***Mode I:*** In this mode, the output voltage is maintained equal to $+V_{dc}$ by turning on the switches $S_1$, $S_5$ and $S_6$. The $-V_{dc}$ level is achieved by turning on the other three switches $S_2$, $S_3$ and $S_4$.

***Mode II:*** In this mode, the output voltage is maintained equal to $+2V_{dc}$ by turning on the switches $S_3$, $S_4$ and $S_5$. Similarly, $-2V_{dc}$ level is achieved by turning on the other switches $S_1$, $S_2$ and $S_6$.

***Mode III:*** In this mode, the output voltage is maintained equal to $+3V_{dc}$ by turning on the switches $S_1$, $S_3$ and $S_5$. Whereas $-3V_{dc}$ level is achieved by turning on the switches $S_2$, $S_4$ and $S_6$.

It can be noticed that a maximum of three switches only in operation for each level generation which results in increased efficiency. Table 1 shows the switching logic of seven-level inverter and their corresponding output voltages. A simple level shifted triangular carrier with Sine Pulse Width Modulation method is used. The control logic can be easily implemented using Xilinx blocks in Matlab software with Spartan 6 FPGA board to generate the control pulses.

**Table 1.** Switching states for level generation

| Level | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
|---|---|---|---|---|---|---|
| $+V_{dc}$ | ON | OFF | OFF | OFF | ON | ON |
| $+2V_{dc}$ | OFF | OFF | ON | ON | ON | OFF |
| $+3V_{dc}$ | ON | OFF | ON | OFF | ON | OFF |
| $0\ V_{dc}$ | ON | ON | ON | OFF | OFF | OFF |
| $0\ V_{dc}$ | OFF | OFF | OFF | ON | ON | ON |
| $-V_{dc}$ | OFF | ON | ON | ON | OFF | OFF |
| $-2V_{dc}$ | ON | ON | OFF | OFF | OFF | ON |
| $-3V_{dc}$ | OFF | ON | OFF | ON | OFF | ON |

## 3. Comparison of Different Seven-Level Inverters

In this section, a detailed comparison of various single-phase seven-level inverter topologies is carried out. In this comparison, the primary focus is on the evaluation of various components such as the number of dc sources, capacitors, diodes, and switching devices. Fig. 3 illustrates the various configurations proposed for single phase seven-level inverter operation for PV applications. Table 2 details all the above-said information in a comprehensive way to recently proposed seven-level inverter topologies.

**Table 2.** Comparison of different seven-level inverter topologies

| Topology | (a) | (b) | (c) | (d) | (e) | Total | Extended ability |
|---|---|---|---|---|---|---|---|
| NPC | 1 | 6 | 0 | 12 | 10 | 29 | Yes |
| FC | 1 | 2 | 5 | 12 | 0 | 20 | Yes |
| CHB | 3 | 3 | 0 | 12 | 0 | 18 | Yes |
| Ref. [17] | 1 | 3 | 0 | 8 | 4 | 16 | Yes |
| Ref. [18] | 1 | 2 | 0 | 9 | 2 | 14 | Yes |
| Ref. [19] | 2 | 0 | 0 | 8 | 0 | 10 | Yes |
| Ref. [20] | 1 | 3 | 0 | 8 | 5 | 17 | No |
| Ref. [21] | 1 | 4 | 0 | 7 | 10 | 22 | Yes |
| Proposed | 1 | 3 | 0 | 7 | 2 | 13 | Yes |

*(a)– Number of sources; (b)–Input capacitors; (c)–Clamping capacitors; (d)–Power switches; (e)–Diodes*

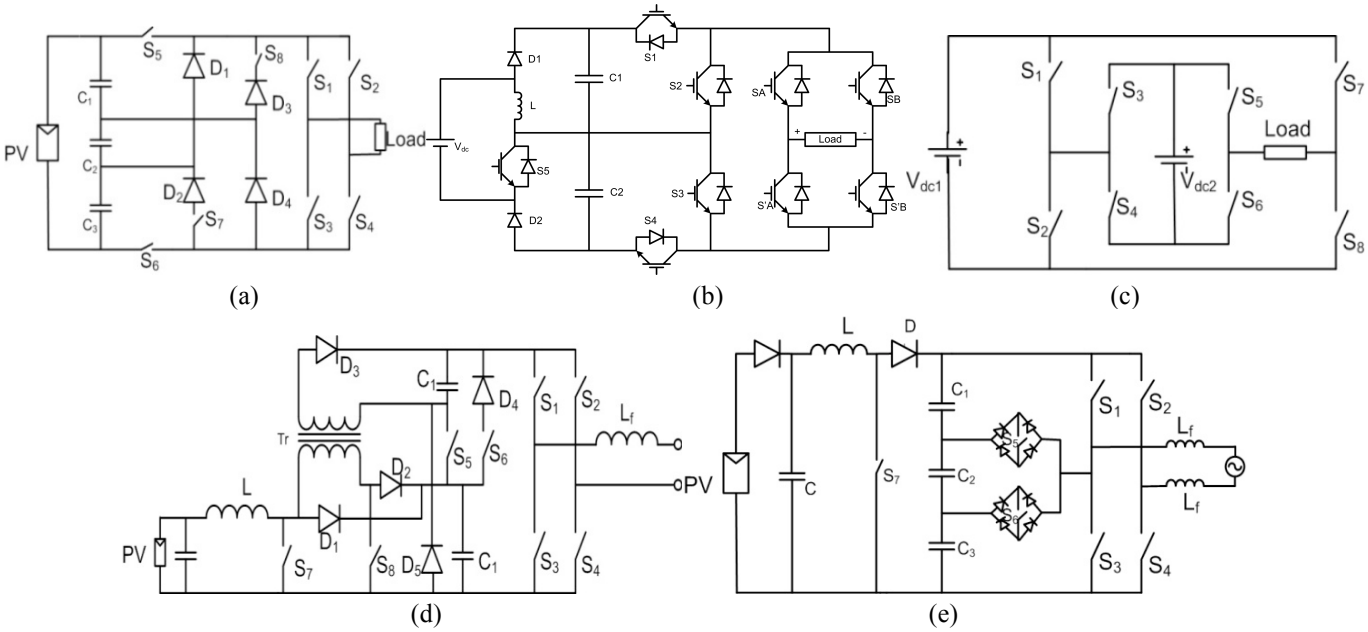



**Fig. 3.** Various seven-level inverter topologies (a) Ref. 17, (b) Ref. 18, (c) Ref. 19, (d) Ref. 20, and (e) Ref. 21.

It can be noticed that, in this comparison, the primary concern given for topologies with single source operation. The proposed topology has least component count as compared to traditional and other seven-level inverter topologies. Moreover, the total number of switching device conduction for every level is lower as compared to the different topologies which result in lower loss and higher efficiency as compared to the other topologies. Moreover, the proposed MLI is modular structure and use of transformer gives isolation for leakage current due to various parasitic elements of the PV panel.

## 4. Results and Discussion

First, the proposed single-phase seven-level inverter is built in Matlab/Simulink environment with the specifications given in Table 3. The performance of the proposed configuration is tested for varying input voltages from 55V to 45V for a constant load of R=200Ω. Switching frequencies of 25kHz and 3kHz are taken for the SEPIC converter and MLI respectively. It can be noticed that from Fig. 4 the desired dc link voltages of $V_{dc1}$ and $V_{dc2}$ are 80V and 160V respectively maintained constant during input voltage changes. The corresponding increase in the duty cycle for the decrease in input voltages shows the better response of the controller. Fig. 5 illustrates the measured seven-level inverter output voltage, filtered output, and the corresponding load current. Figs. 6(a) & (b) illustrates the frequency spectrum of the seven-level inverter output voltage with and without a filter. It can be noticed that the dominating harmonics at the 60th order is effectively filtered out and the lower order harmonics are also eliminated. Thus the %THD of the voltage waveform is reduced from 24.26% to 1.85%.

**Table 3.** Simulation and experimental parameters

| Parameters | Values |
|---|---|
| Vin | 40V - 60V |
| Vdc1, Vdc2 | 80V, 160V |
| L | 500 µH |
| C | 100 µF |
| C1, C2 | 1000 µF |
| Switching frequency of SEPIC converter | 50 kHz |
| Switching frequency of 7-level inverter | 3 kHz |
| Fundamental frequency | 50 Hz |
| Modulation index, Ma | 0.9 |
| Filter Lf, Cf | 4 mH, 25 µF |
| Load | 100 Ω - 200 Ω |

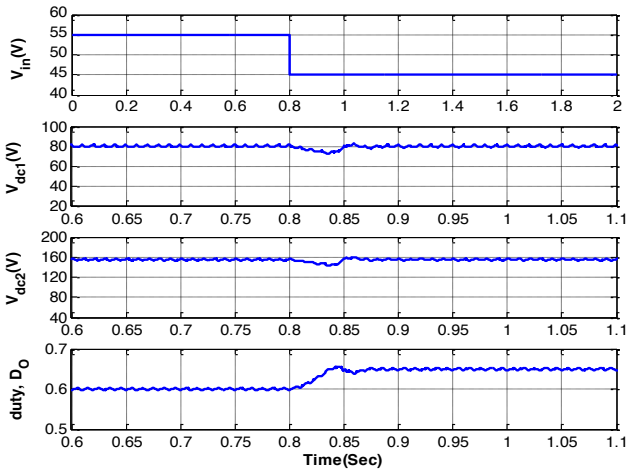



**Fig. 4.** Simulation results of dc-link voltages and duty cycle under input voltage changes.

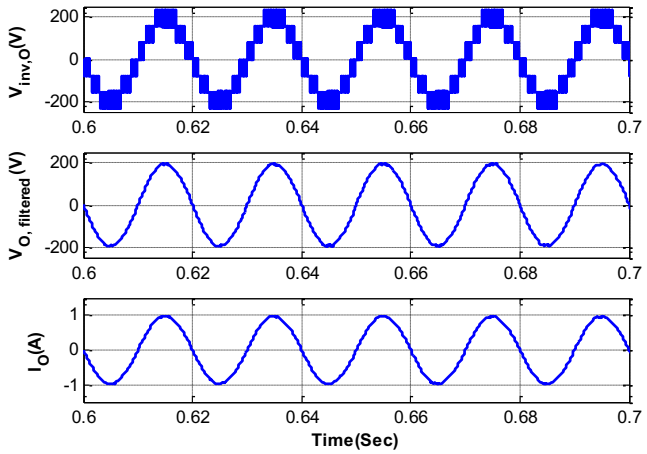
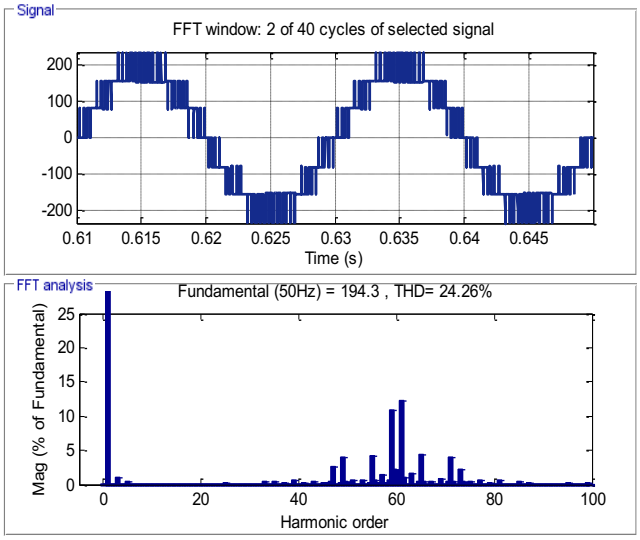
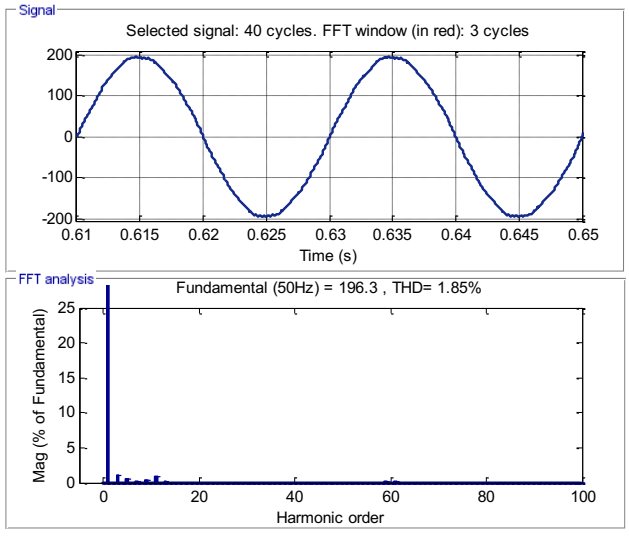



**Fig. 5.** Simulation results of seven-level inverter output voltage, filtered output voltage and load current for R=200Ω.




(a)




(b)

**Fig. 6.** FFT spectrum of inverter output voltage waveform (a) without filter (b) with filter.

In order to validate the concept, a low power/voltage prototype model is developed with the available facilities in the laboratory. Fig. 7 depicts the developed experimental setup with various components consists of the power circuit, driver circuit, etc. The power circuit is built with IRF460 Mosfet switches, and TLP250 ICs are used for driver circuits. The other component values are selected for experimentation is similar to simulated parameters. The closed-loop controller for the front end SEPIC inverter is implemented using DSP2812 in real time workshop. Figs. 8(a) & (b) illustrates the procedure for built of PWM pulse generation and the PI controller developed in Matlab using DSP 2812 target [22]. The controller pulses for MLI is generated using Xilinx blocks in Matlab software and Spartan 6 FPGA board. The response of the proposed configuration is measured through mixed signal oscilloscope 3034 under different testing conditions.

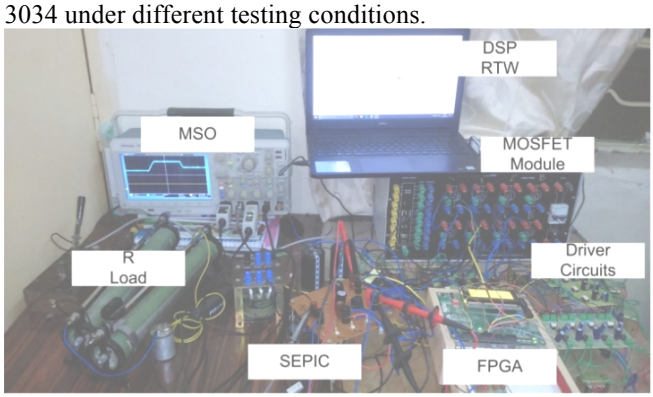
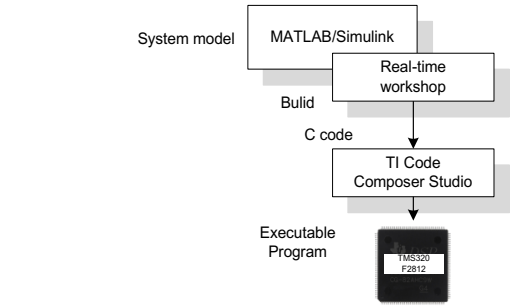
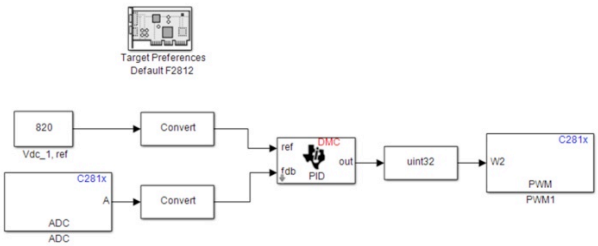



**Fig. 7.** Experimental setup.




(a)




(b)

**Fig. 8.** (a) RTW DSP implementation (b) Close loop controller with DSP Target.

Fig. 9(a) shows the measured seven-level inverter output voltage, filtered output, and their corresponding load current. Fig. 9(b) shows the response of inverter output voltage, dc link voltage $V_{dc1}$ during load rising conditions. Similarly, Fig. 9(c) shows the response of controller during load falling conditions. It can be noticed that the dc link voltage and the output voltage is always maintained constant either load

increases or decreases. This shows the performance of the developed controller in the closed loop environment, and it's better controlling action during load changes. In addition, the performance of the proposed topology is tested during input voltage changes from 40V to 50V and then reduces from 50V to 47V are shown in Figs. 9(d) & (e). It can be observed that both the dc link voltages $V_{dc1}$ & $V_{dc2}$ are maintained constant as 80V and 160V respectively by adjusting the duty cycle of the front end inverter. Fig. 9(f) ensures the continuous input current operation of the SEPIC converter. Finally, Figs. 9(g) & (h) shows the harmonic spectrum of seven-level inverter output voltage and filtered output voltage waveforms with the THD of 23.78% and 5.06% which are close to the simulation results and within the IEEE-519 standards. This shows the capability of the proposed topology is more suitable for Photovoltaic/ Fuel cell based low power/voltage applications.

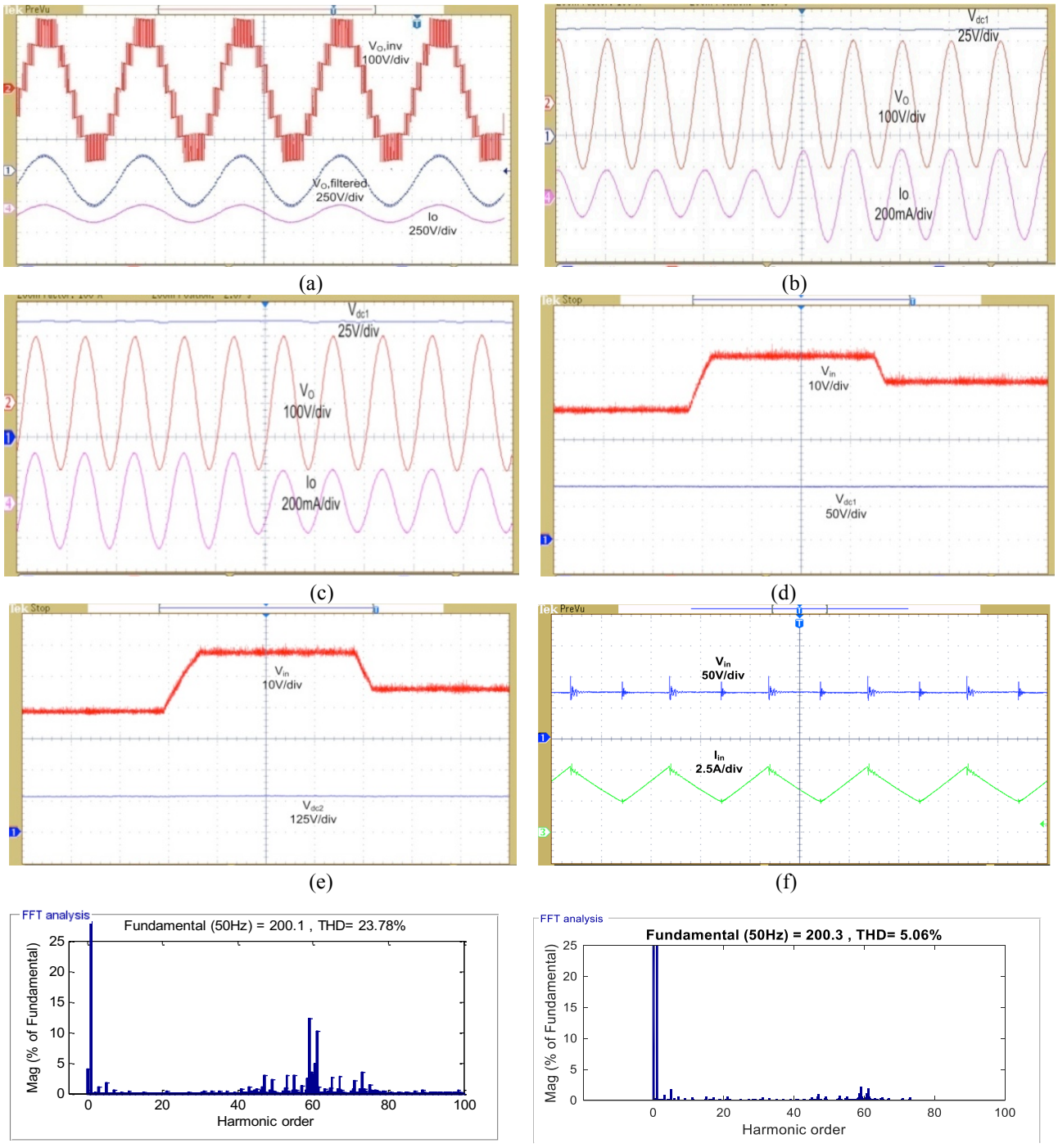



**Fig. 9.** Experimental results of (a) Seven-level inverter output voltage, filtered output voltage and load current, (b) Step response of increase in load current, (c) Step response of decrease in load current, (d) Changes in input voltage and corresponding dc-link voltage $V_{dc1}$, (e) Changes in input voltage and corresponding dc-link voltage $V_{dc2}$, (f) input voltage and current, and (g)-(h) Frequency spectrums of seven-level inverter output voltage and filtered output voltage waveforms from CSV file.

## 5. Voltage Quality and Efficiency Analysis

The suitable LC filter design decides the voltage quality of the inverter output waveform. However, the increase in size and volume determines the cost and weight of the filter components. The selection of cut-off frequency (*fc*) is carried out by using the following expressions,

$$f_C = \frac{1}{2\pi\sqrt{LC}}(Hz) \quad (4)$$

where $L$ is the inductor and $C$ is the capacitor.

The size of the LC filter components can be minimized for the reduction in % total harmonic distortion(THD) of the inverter output voltage while increasing the output voltage levels. Also in MLIs, the increase in output voltage is decided by the corresponding modulation index ($M_a$). For that, the following expression is used to determine the %THD theoretically which is given in [18];

$$THD_{up}(M_a, N_L) = 57.7/M_a/(N_L - 1)\% \quad (5)$$

Where $N_L$ is the (non-negative) level output. Fig. 10 illustrates the calculated %THD of the inverter output voltage waveform for different $M_a$ and different output voltage levels. It can be observed that the increase in output voltage results in a reduction in the %THD output and size of the filter components. Moreover, the comparison Table 2 shows the proposed configuration has lower parts count. This results in overall reduction in size. Fig. 11 depicts the measured efficiency curve for varying loads by considering the appropriate resistance values of the various components in PSIM Thermal Module.

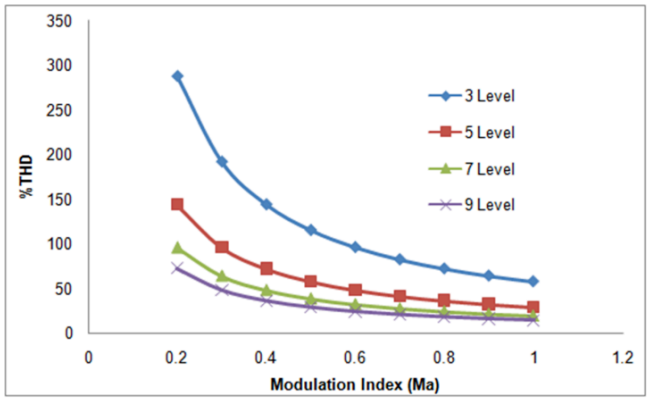



**Fig. 10.** %THD for 3, 5, 7 & level output voltage waveforms.

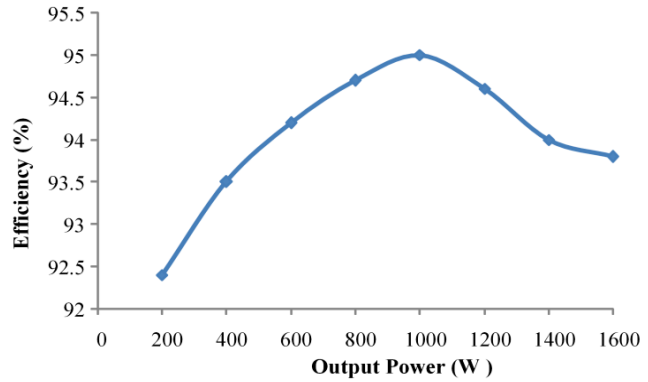



**Fig. 11.** Efficiency curve.

The conduction loss and switching loss of the Mosfet devices are estimated with the general expressions given in Ref. [23].

$$\text{Efficiency}(\%) = \frac{P_{out}}{P_{out} + P_{loss}} * 100 \quad (6)$$

It can be noticed that the proposed configuration can achieve the maximum of 95% with an increase in output voltage quality. Further, it can be enhanced with the selection of low-on state resistance switches.

## 6. Conclusions

A new configuration of SEPIC based seven-level inverter is presented for low power/voltage renewable applications. The proposed configuration has owned its advantages of reduced device counts and lower number of device conduction for each level generation. This enables the higher efficiency of the proposed configuration as compared to the other seven-level topologies. For that, a detailed comparison of various topologies is presented. The simulation results are good agreement with the experimental results. This shows the capability of the proposed configurations and can be extended for photovoltaic/fuel cell based power supply system.

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